저전력, 저잡음, 넓은 동적범위의 바이오임피던스 판독회로 설계

손현우

경상국립대학교 IT공과대학 전자공학부

Outline

- Introduction of Bioimpedance (BioZ)
- BioZ Readout Overview
- Proposed BioZ Readout IC
- Measurement results
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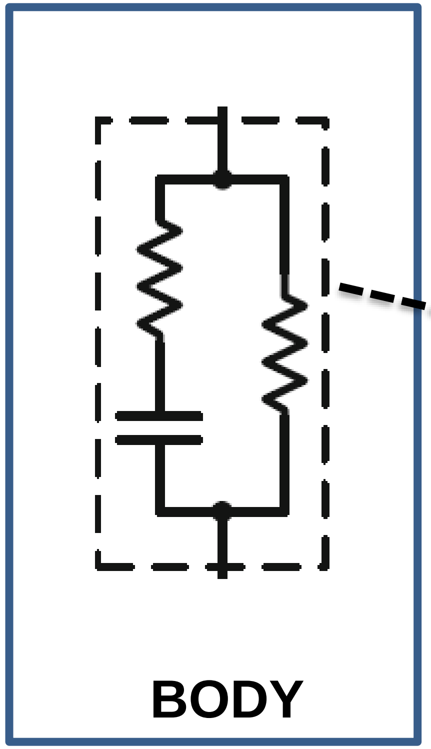
Bioimpedance (BioZ)

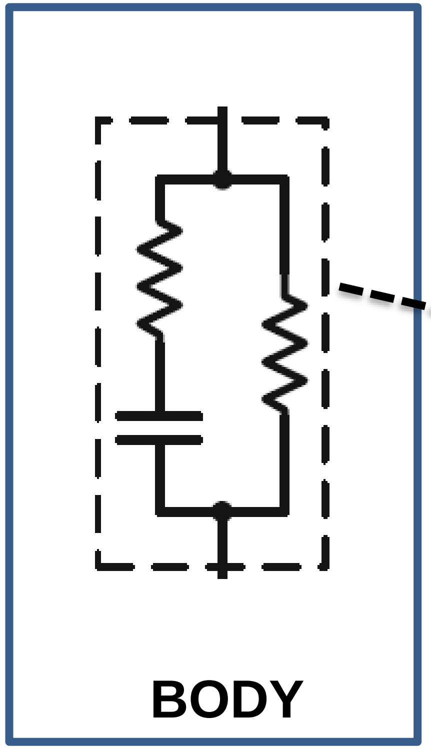


Z_{BioZ} (100Ω-1kΩ)[1] + ΔZ_{BioZ} (0.1Ω-10Ω)[1]

[1]S. Kim, ISSCC, 2013

- 인체: 조직 구성 (지방, 근육 등) 에 의해 영향 받는 전기 전도체

Bioimpedance (BioZ)

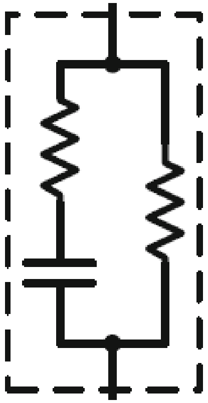


Z_{BioZ} (100Ω-1kΩ)[1] + ΔZ_{BioZ} (0.1Ω-10Ω)[1]

[1]S. Kim, ISSCC, 2013

- Z_{BioZ}: 체성분 (지방, 근육, 뼈 등)
- ΔZ_{BioZ}: 호흡, 심장박동 ➔ BioZ 변화

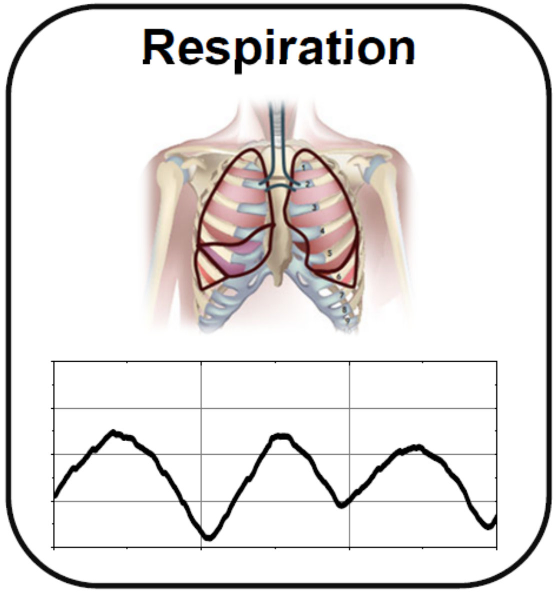
BioZ Application

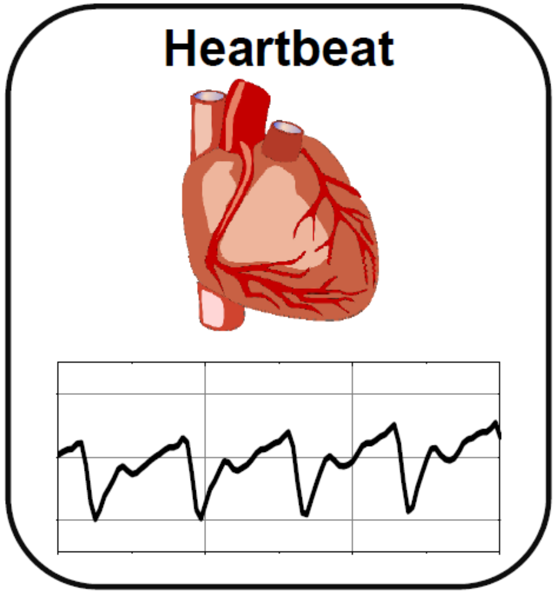


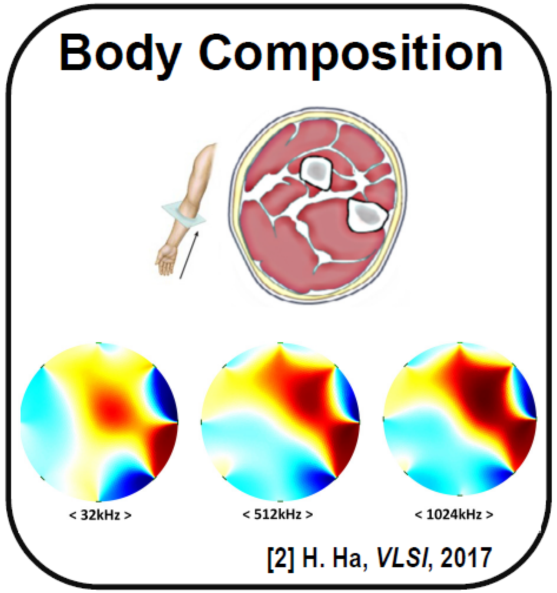
$$\boxed{Z_{BODY}} + \boxed{\Delta Z_{BODY}}$$

Vital sign : 호흡 or 심장박동 (< 100mΩ, few-mΩ/√Hz)[1]

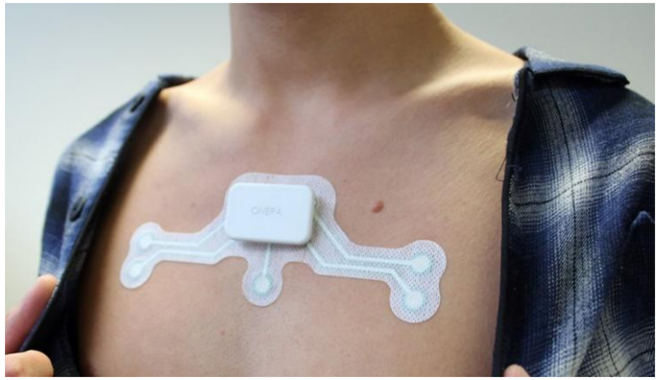
체성분 분석 or 전기임피던스영상법



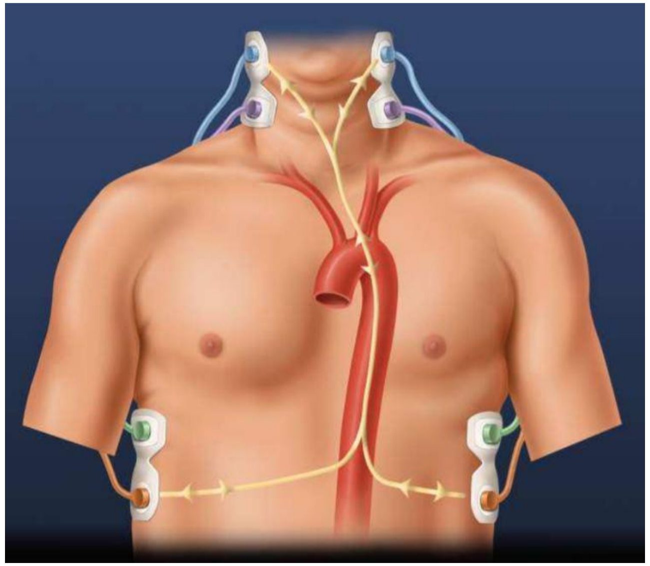




Motivations



Onera BioZ Patch

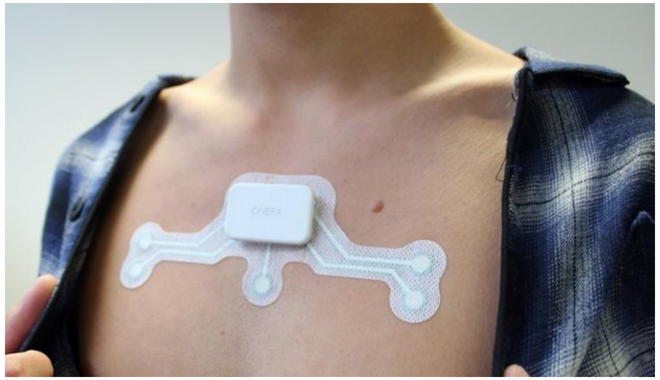


BioZ® Cardio

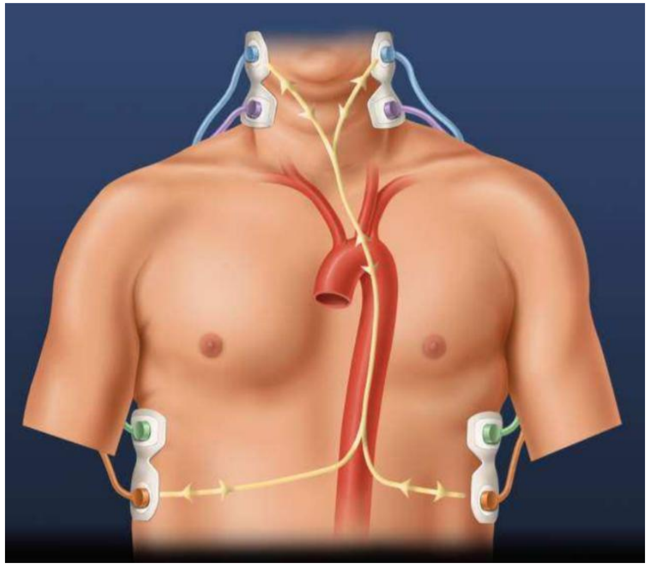
AURA Device

- **BioZ 웨어러블 기기에서 널리 활용**
- **BioZ 변화는 vital signals 을 반영**

Motivations



Onera BioZ Patch



BioZ® Cardio

AURA Device

- 더 적은 전력소모 → 배터리 수명 연장
- 더 낮은 잡음 (*1/f* 잡음) → 높은 **signal quality**

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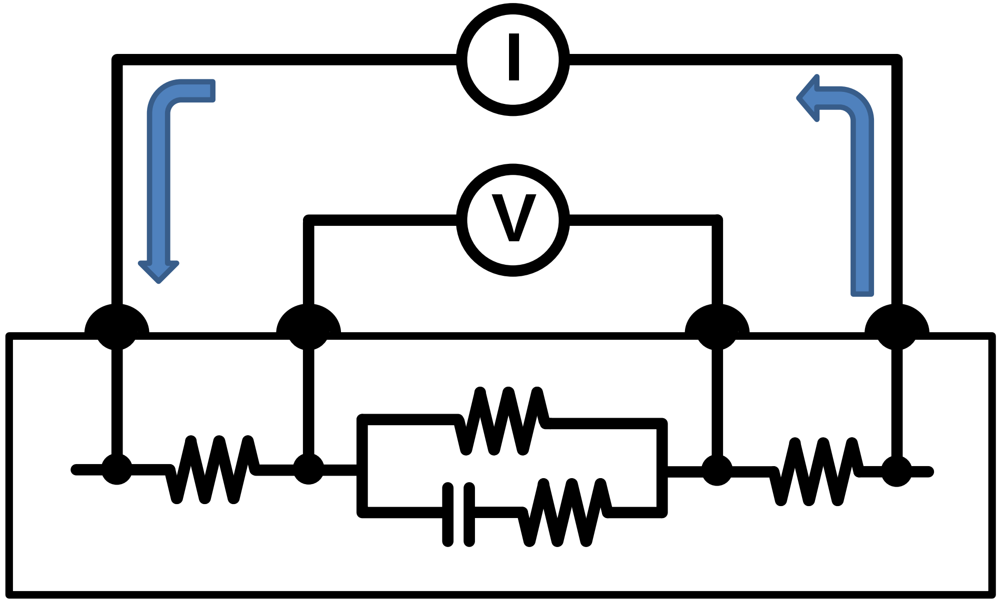
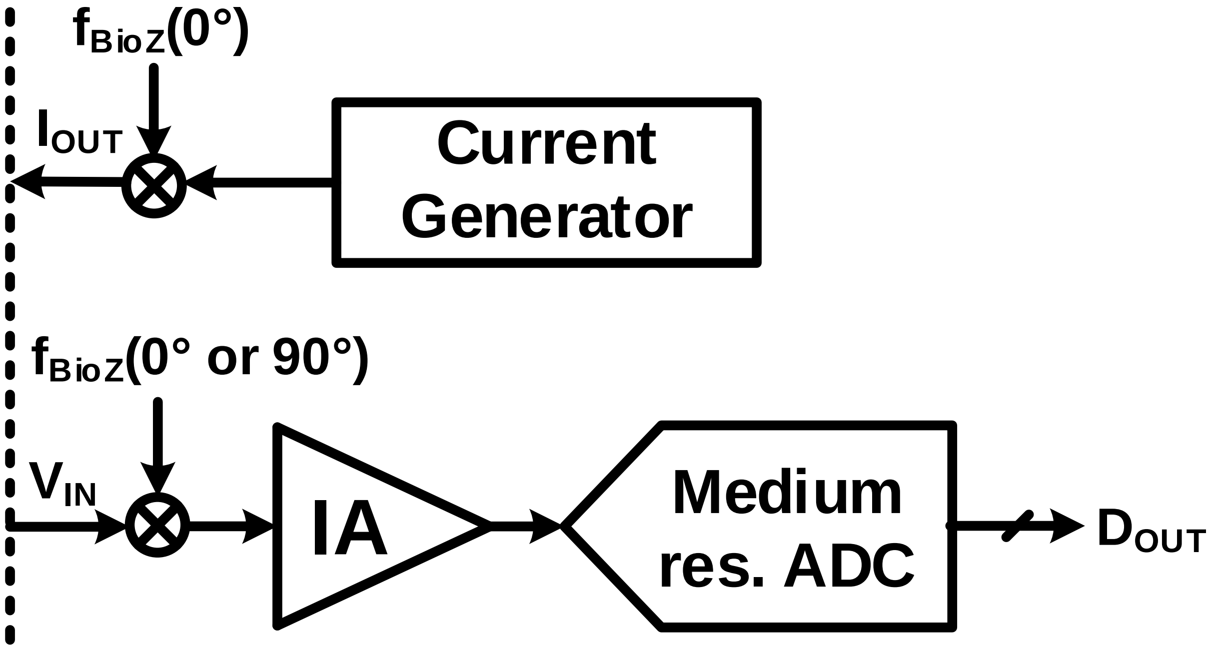
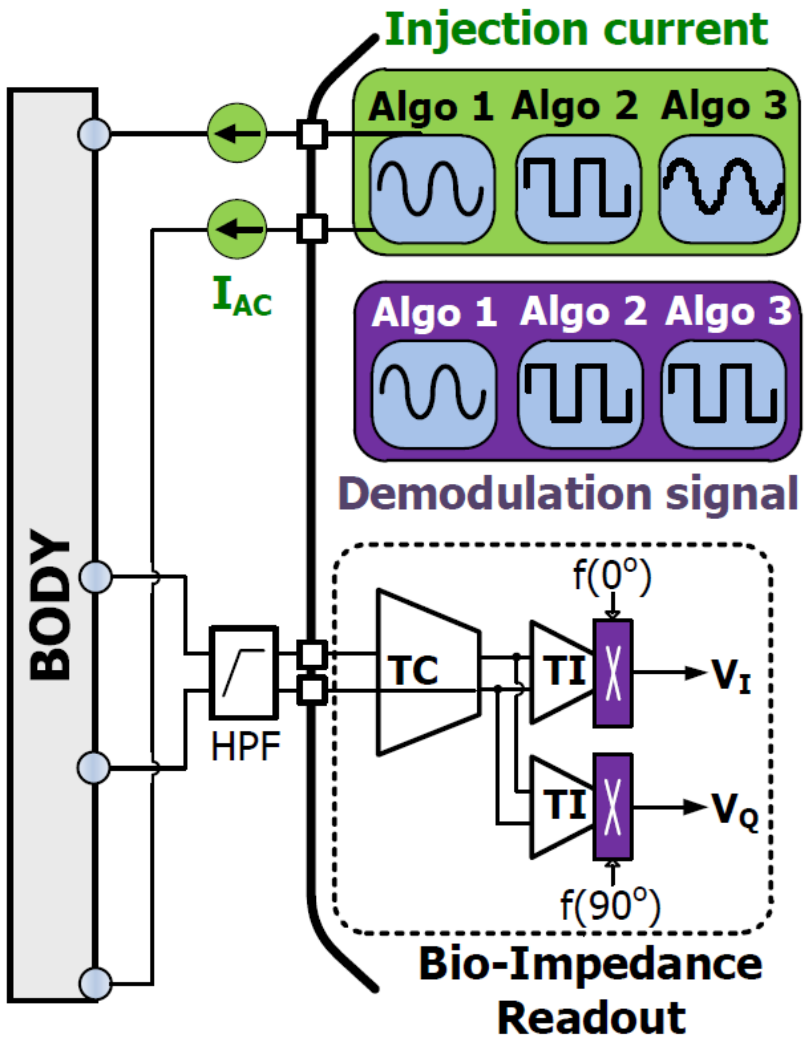
Conventional BioZ Measurement





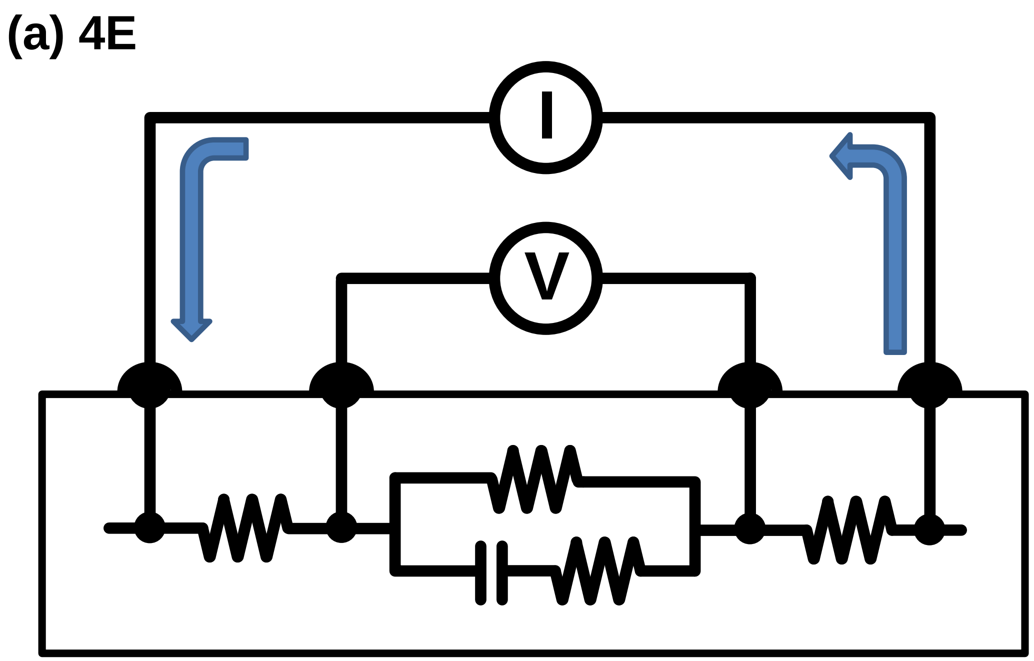
- AC 전류 주입 후 전압 측정
- Instrumentation amplifier (IA) + ADC architecture

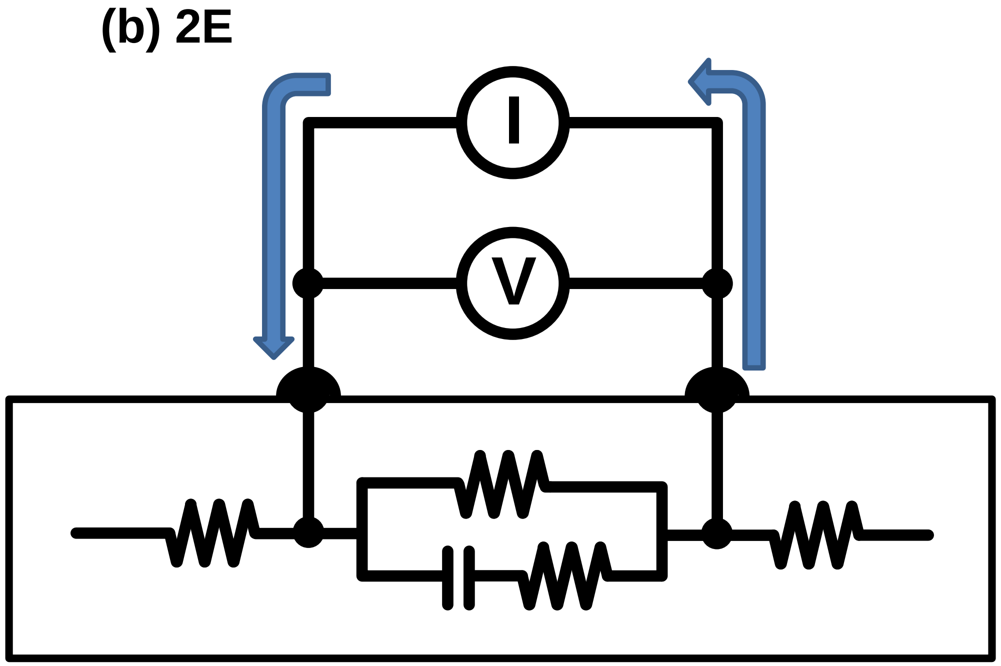
Current Modulation for BioZ Measurement



- **Pure sine wave**
  - ✓ 낮은 harmonic distortion
  - × mWs of power
- **Square wave**
  - ✓ µW-range power
  - ✓ 간단한 design
  - × odd harmonics 으로 인한 오류
- **양자화된 sine wave**
  - ✓ µW-range power
  - ✓ harmonics에 의한 오류 감소
  - × LUT, DAC, CTRL logic 필요

Two-Electrode (2E) Setup

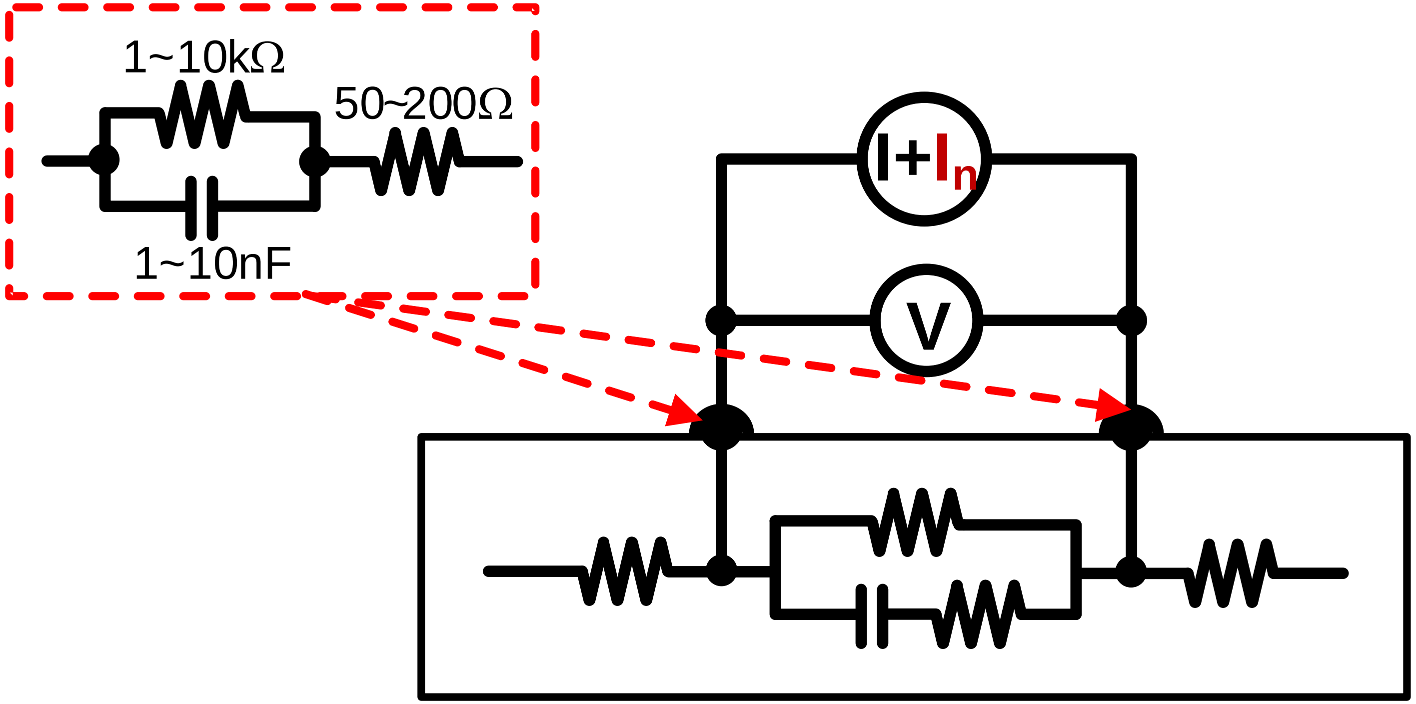




- 두 개의 전극을 공유
- 절대적인 **BioZ** (**$Z_{BioZ} + \Delta Z_{BioZ}$**) 측정을 위한 **4E setup**
- 상대적인 **BioZ** 변화 (**ΔZ_{BioZ}**) 측정을 위해 **2E setup** 적용가능

2E BioZ Measurement

$Z_{ELEC} >> Z_{BioZ}$



✓ 복잡도 감소

✓ 더 편안함

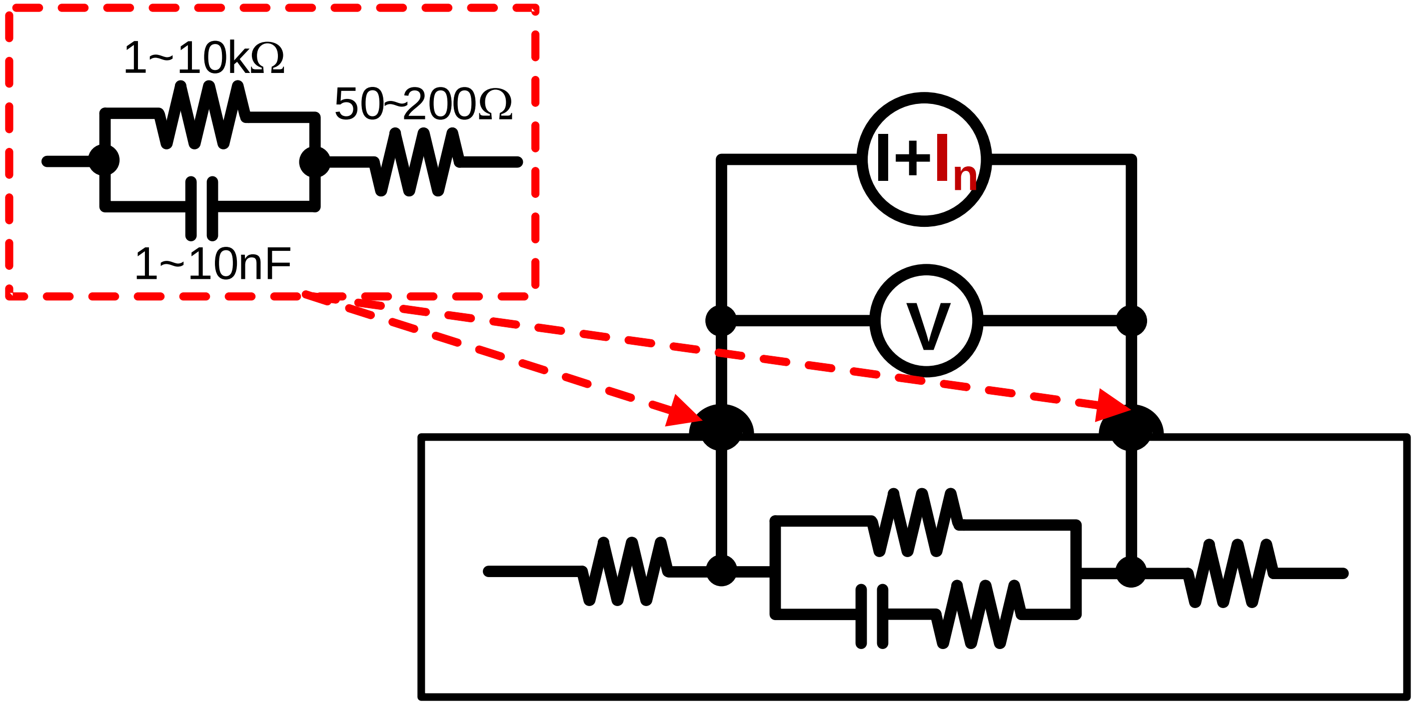
✓ 더 낮은 비용

× 큰 입력 임피던스 값 **(~20kΩ),** 그러나 ΔZ_{BioZ}는 호흡의 경우 수 **Ω** 그리고 심장박동의 경우 **<1 Ω →** 넓은 동적범위 필요

× 큰 Z_{ELEC} 전류 잡음을 입력 전압 잡음으로 변환 **→** 입력 잡음 증가

2E BioZ Measurement

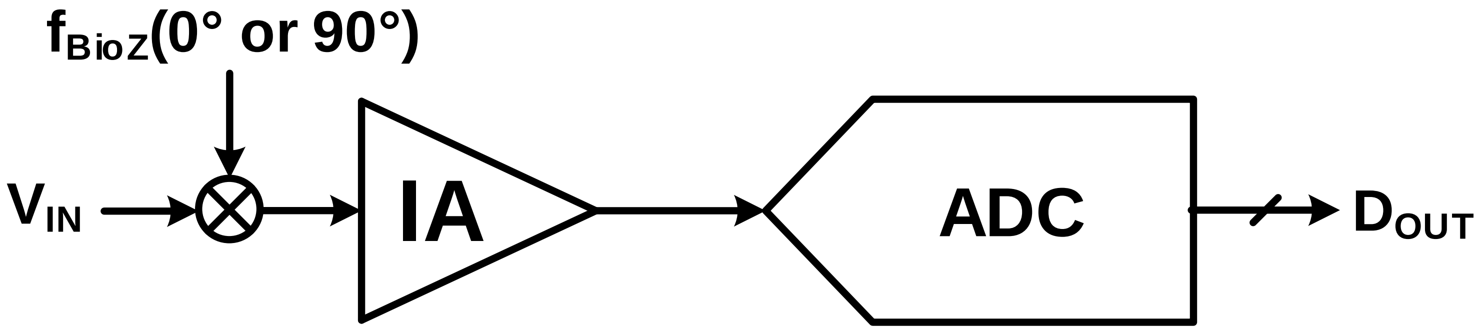
$Z_{ELEC} >> Z_{BioZ}$



- ✓ 복잡도 감소
- ✓ 더 편안함
- ✓ 더 낮은 비용

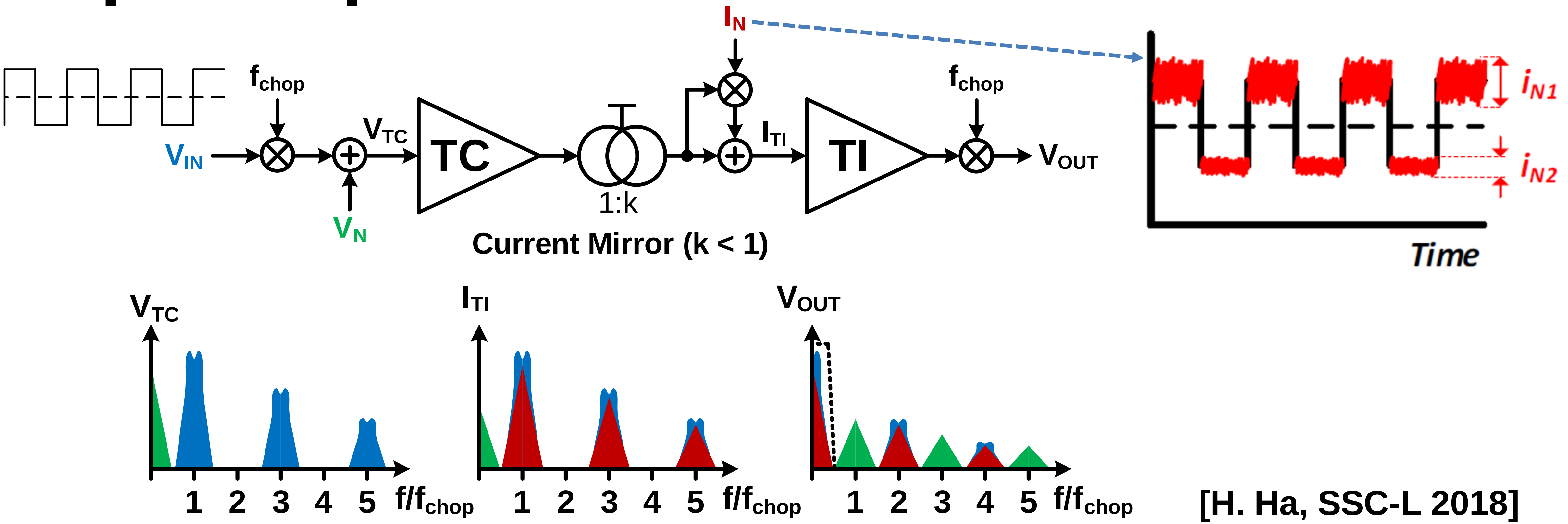
- 저전력, 저잡음, 넓은 동적범위를 갖는 판독회로 필요

Conventional Approach w/ 2E Setup



- **고 이득 IA (> 40dB) + 중간 해상도의 ADC**
  - ✓ ADC의 잡음 필요 성능 완화
  - × 큰 Z_{ELEC} 와 고 이득 IA로 인한 포화문제
- **저 이득 IA + 고 해상도의 ADC**
  - ✓ 고 해상도 ADC의 사용으로 포화문제 방지
  - × IA 와 ADC 모두 저 잡음을 얻기 위해 높은 전력소모 필요

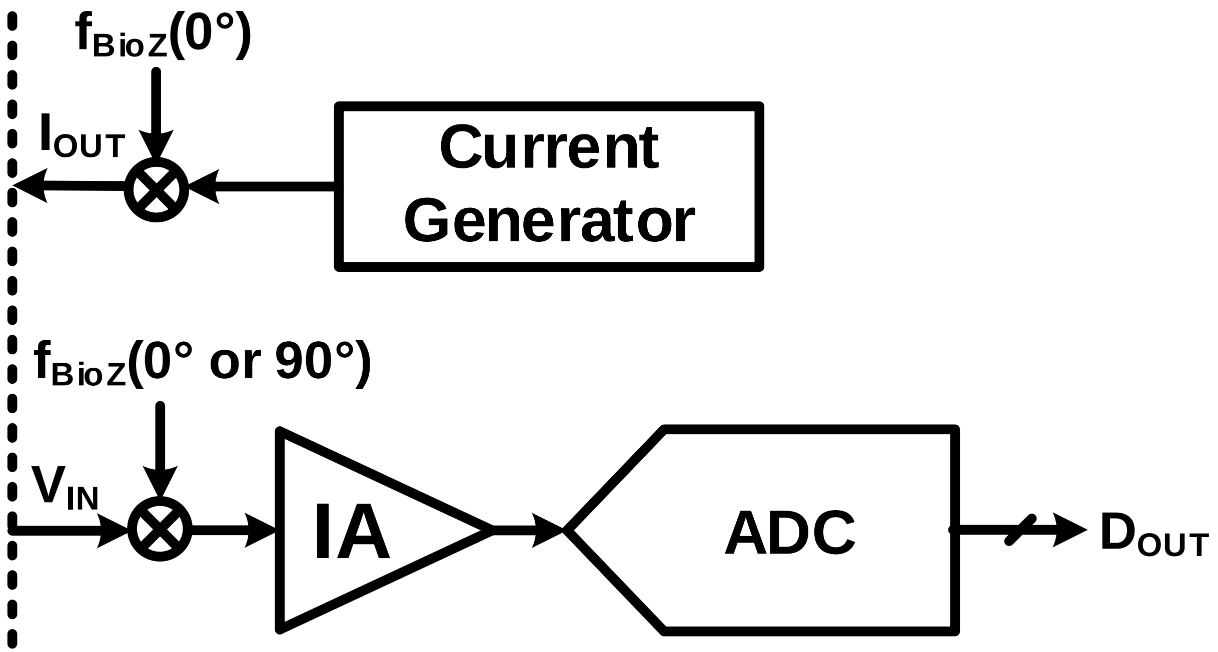
Input-Dependent Noise



[H. Ha, SSC-L 2018]

- **Chopper-stabilized current-balancing IA**
  - ✓ 저 잡음, 높은 전력 효율, 높은 입력 임피던스
  - × 2E setup에서 큰 입력 전압으로 인한 잡음 변조로 SNR 제한

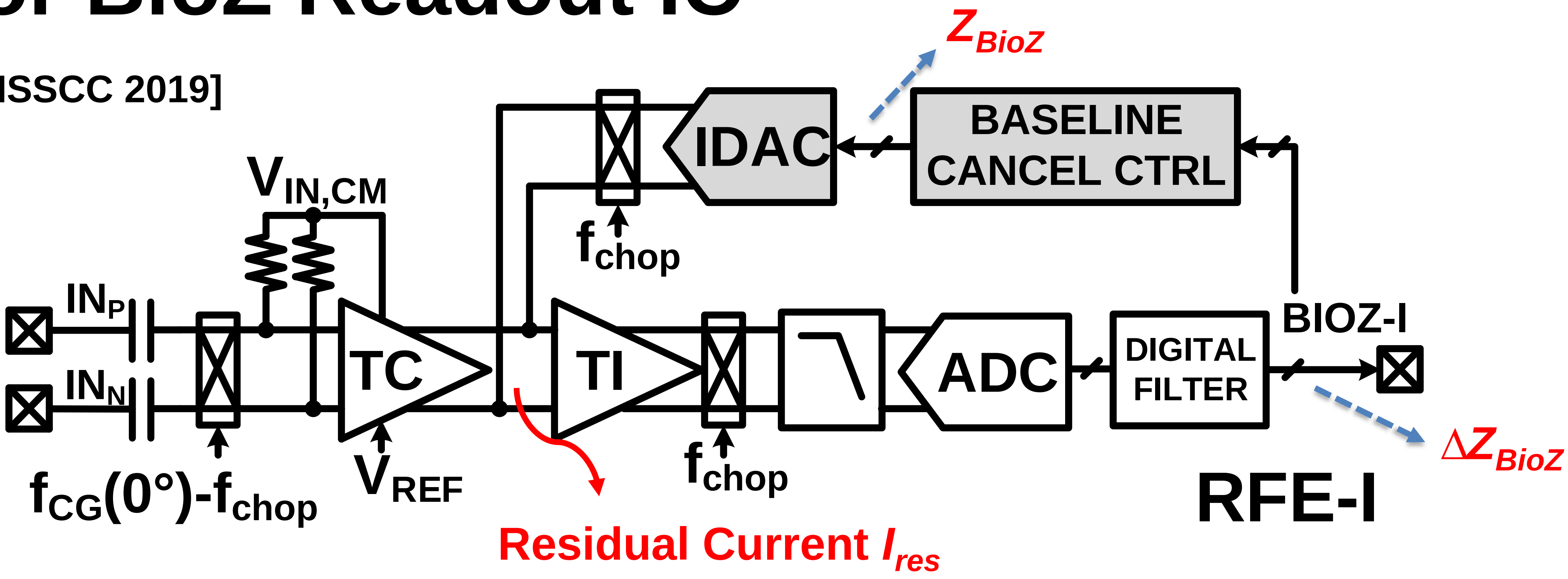
Requirements for 2E BioZ Measurement



- 넓은 동적범위
- 저 잡음 current generator
- 저 잡음 (input-dependent noise & *1/f* noise) 판독회로

Prior BioZ Readout IC

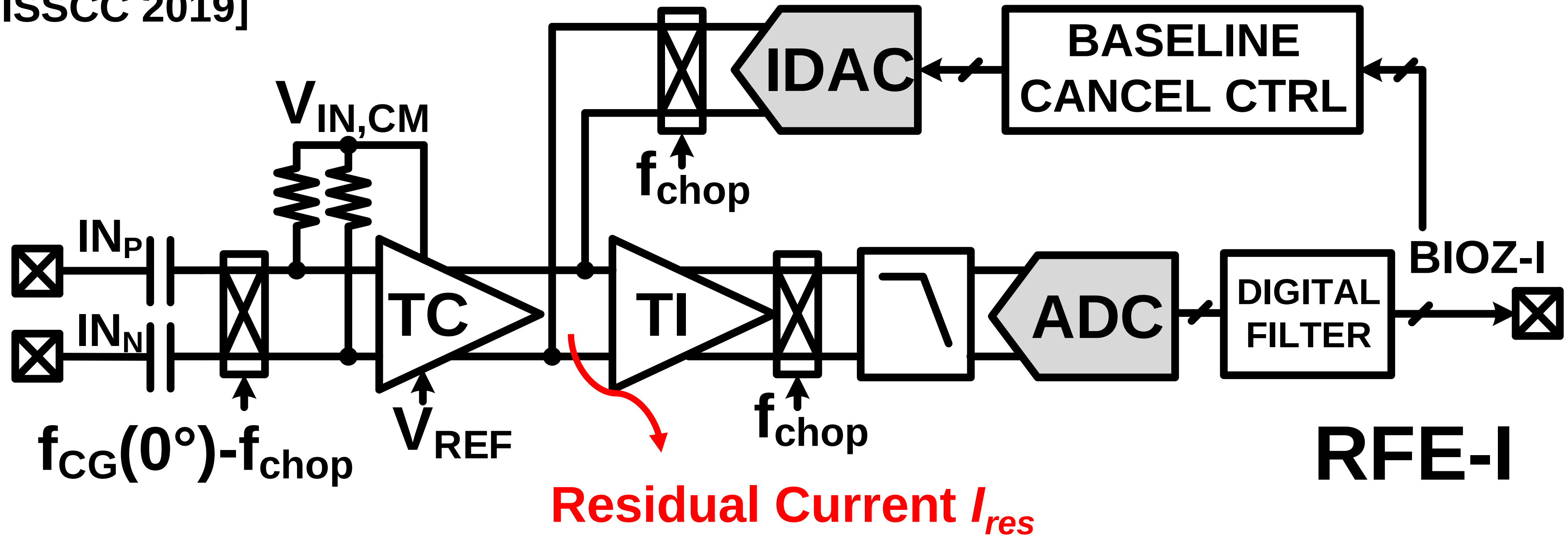
[H. Ha, ISSCC 2019]



- **baseline cancellation loop을 이용한 IA + ADC 구조**
  - ✓ coarse / fine 변환을 이용하여 포화없이 넓은 동적범위
  - ✓ correlation 을 이용하여 I_{REF} 잡음 상쇄 및 input-dependent noise 감소

Prior BioZ Readout IC

[H. Ha, ISSCC 2019]



- ✗ finite I_{RES}로 인한 잔여 input-dependent noise
- ✗ coarse / fine 변환 사이의 gain mismatch
- ✗ 느린 loop bandwidth (~0.5s)

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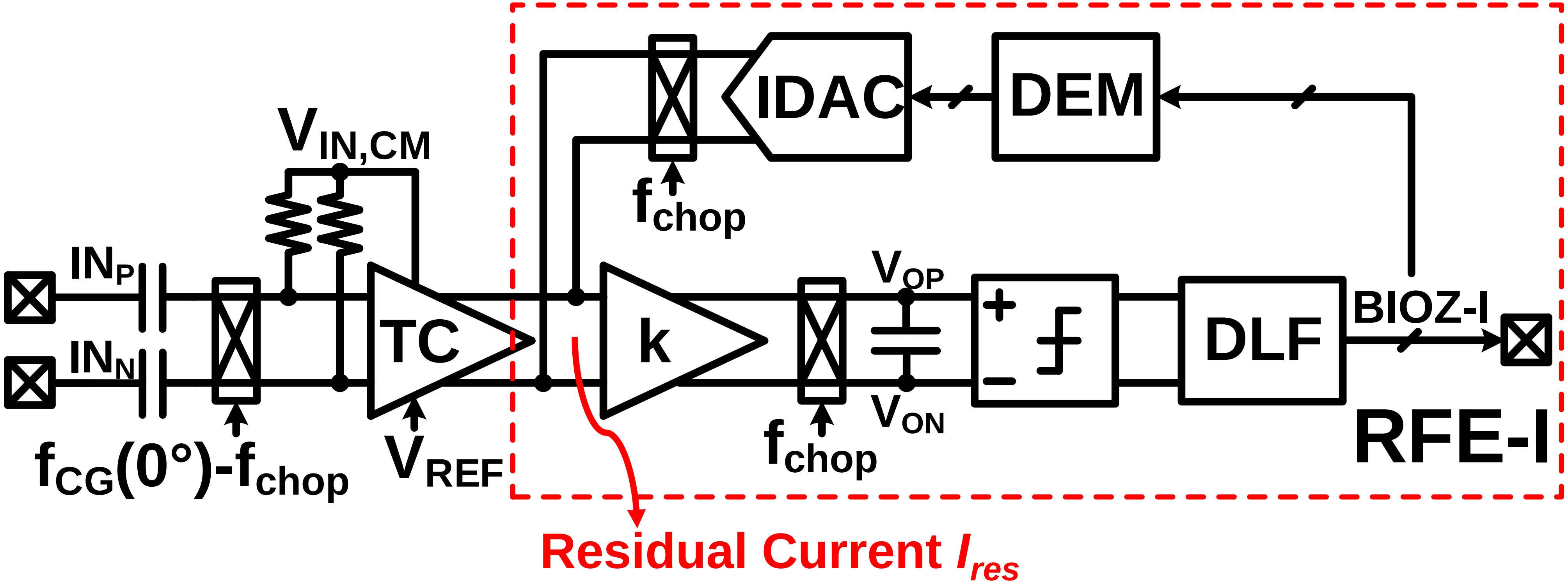
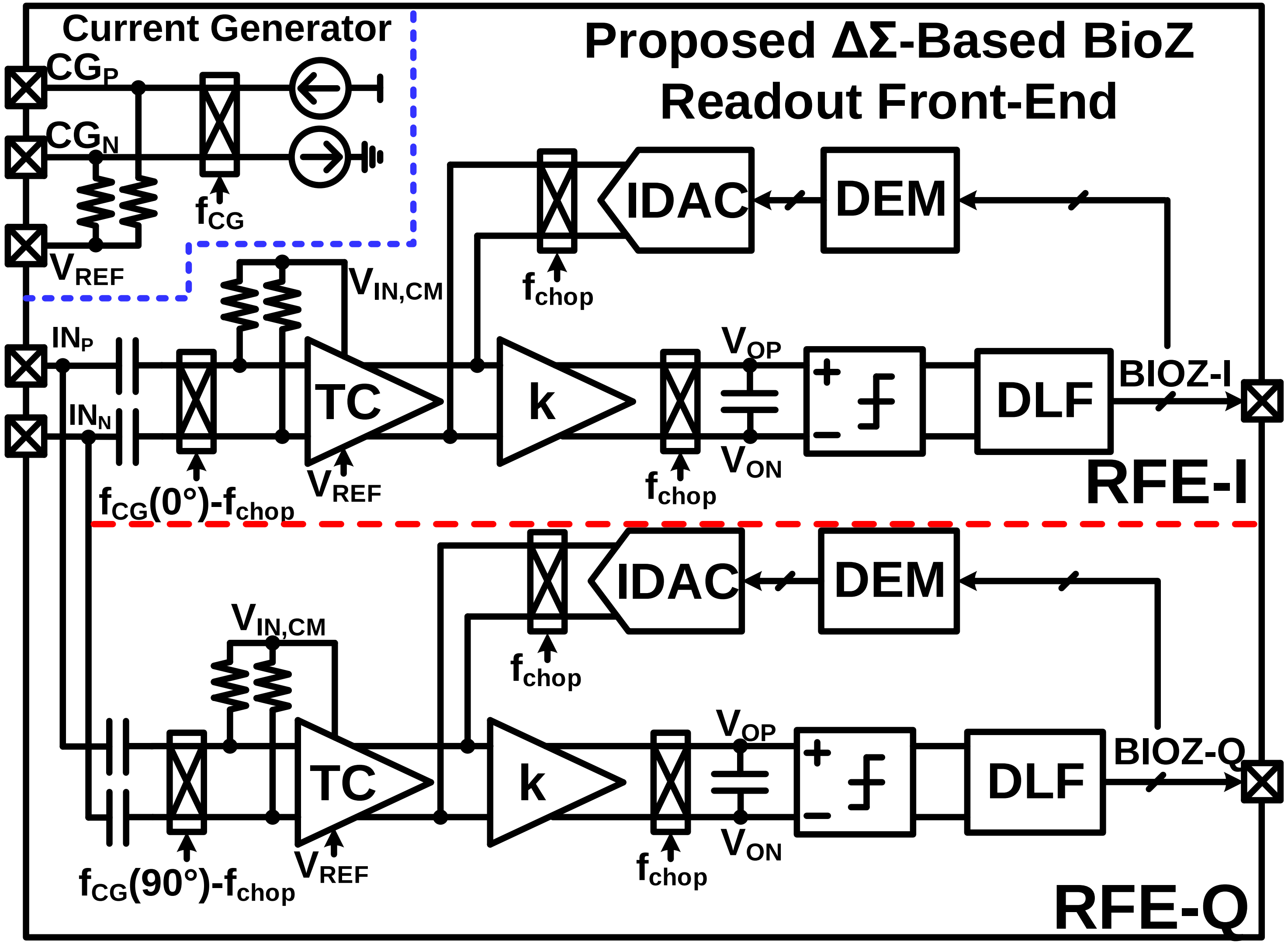
Proposed BioZ Readout IC (I-Phase)



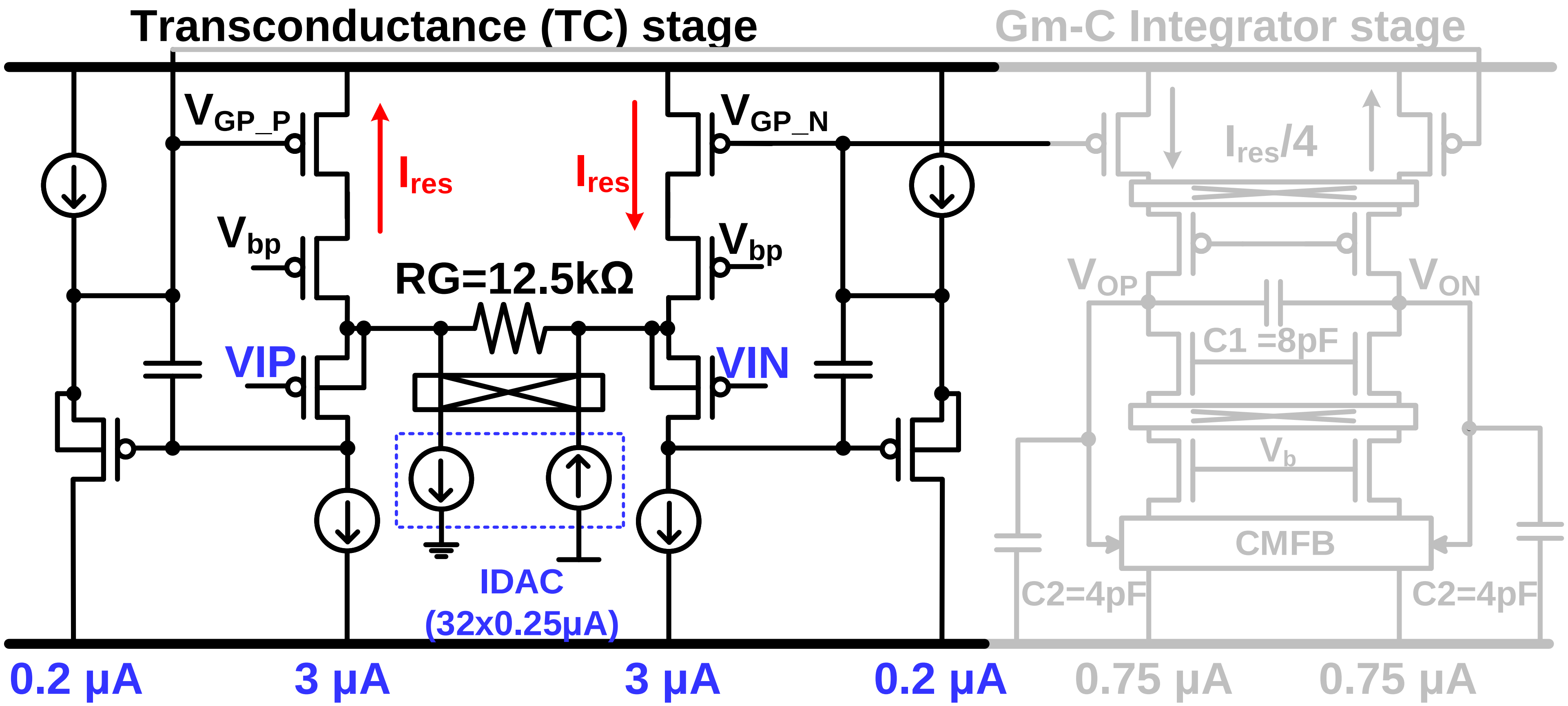
- ✓ I_{res} 최소화하기 위한 DLF을 이용한 ΔΣ구조 → 더 낮은 input-dependent noise
- ✓ DEM을 적용한 하나의 DAC → 선형성 향상
- ✓ Continuous-time 1차 noise-shaping → 더 높은 SNQR & 에너지 효율
- ✓ CG & IDAC 에 I_{REF} 공유하여 I_{REF} noise 상쇄

System Diagram



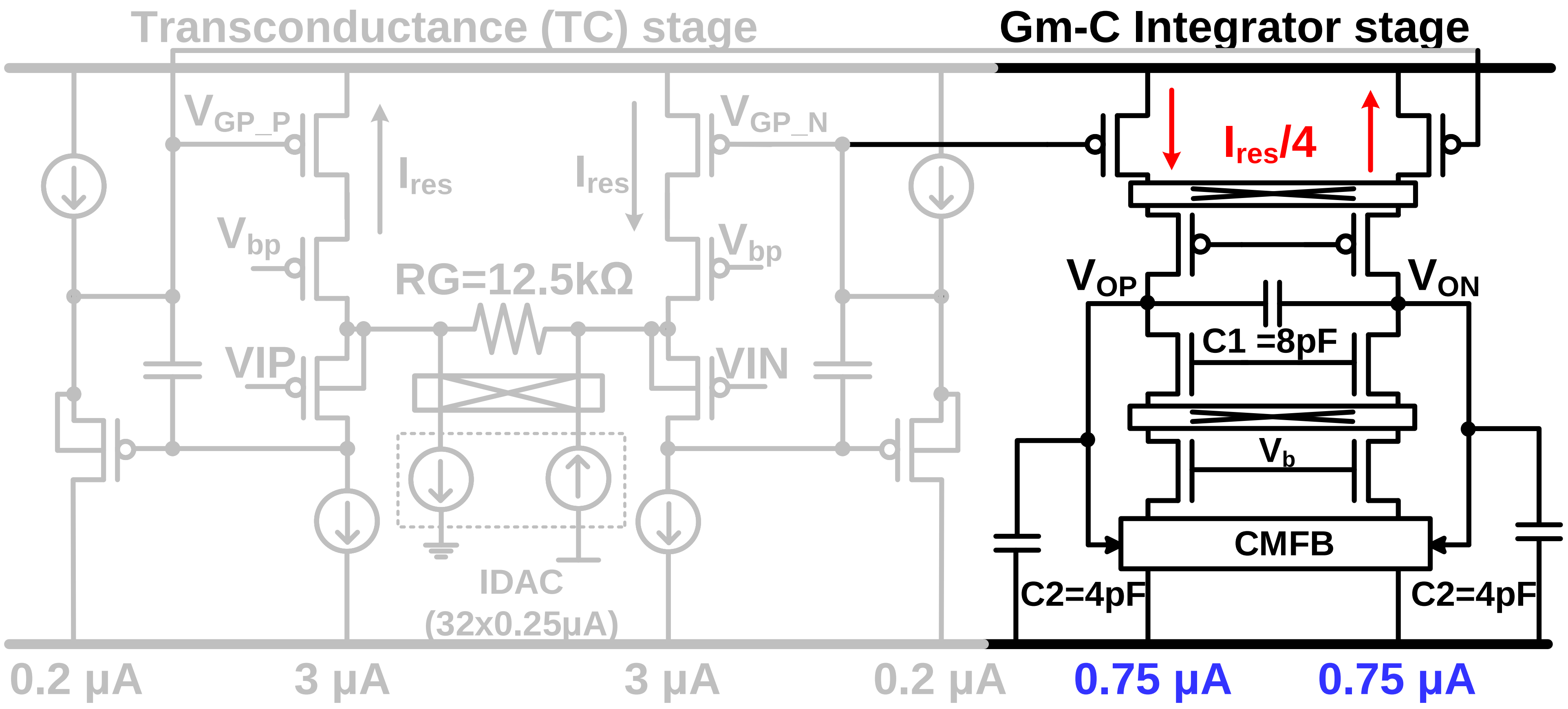
- ΔΣ기반 토폴로지
- CG, IREF, IDAC에 DEM 적용
- DLF을 이용한 다중 비트 quantizer
- I & Q 측정

TC (V-I Conversion)



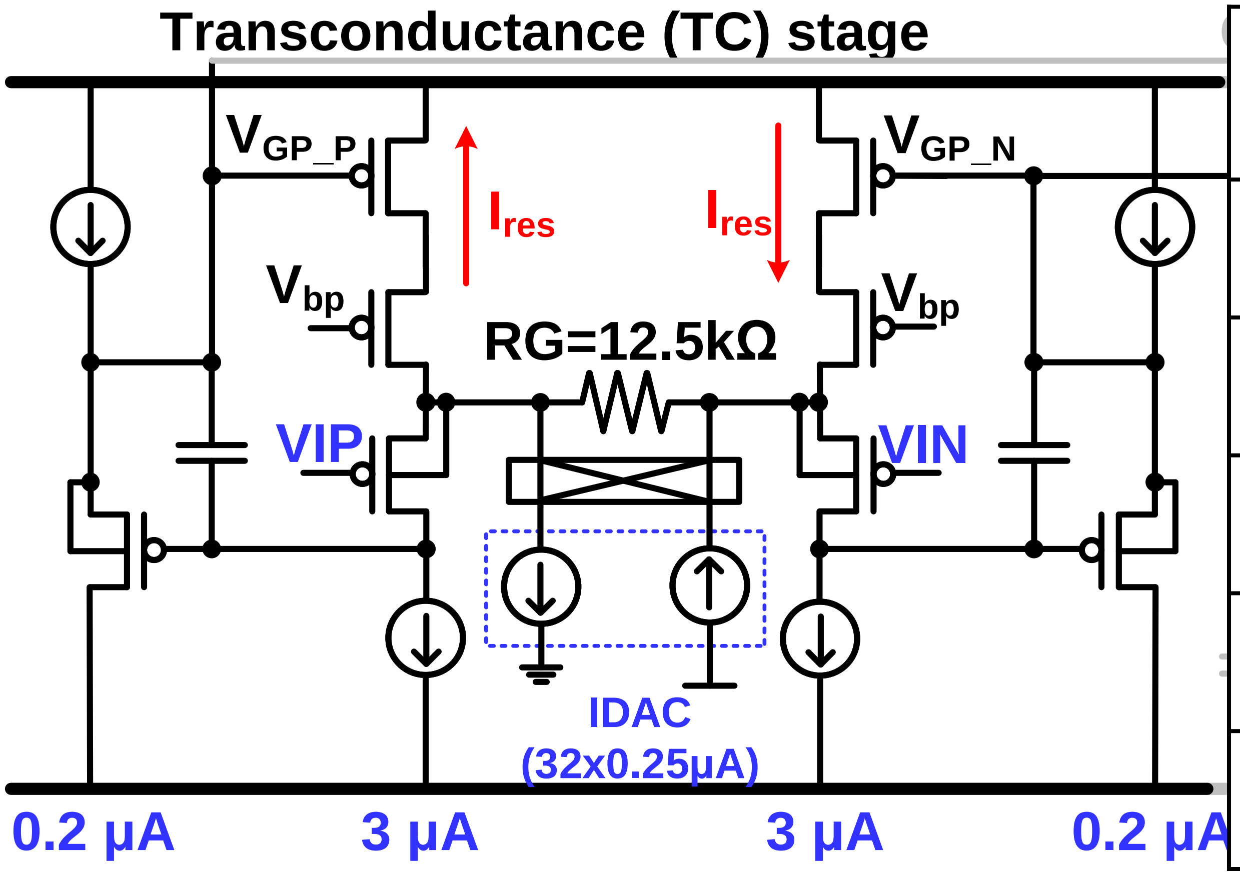
- 주된 열 잡음 (input pair and RG)
- 최대 입력 신호 진폭:100 mV_{pk}

Gm-C Integrator



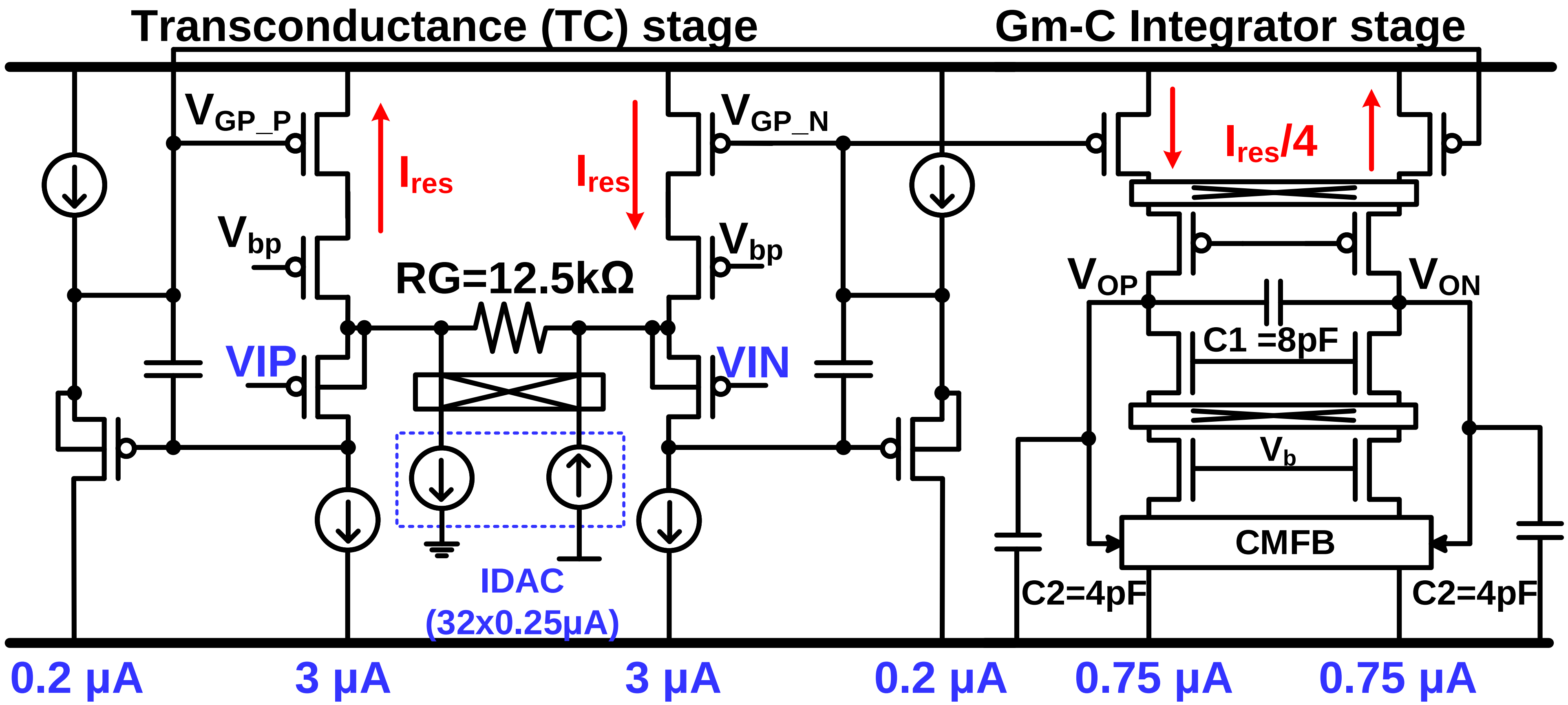
- 저전력 을 위해 ¼ I_{RES} 복사 및 **Gm-C integrator**

TC Stage Stability



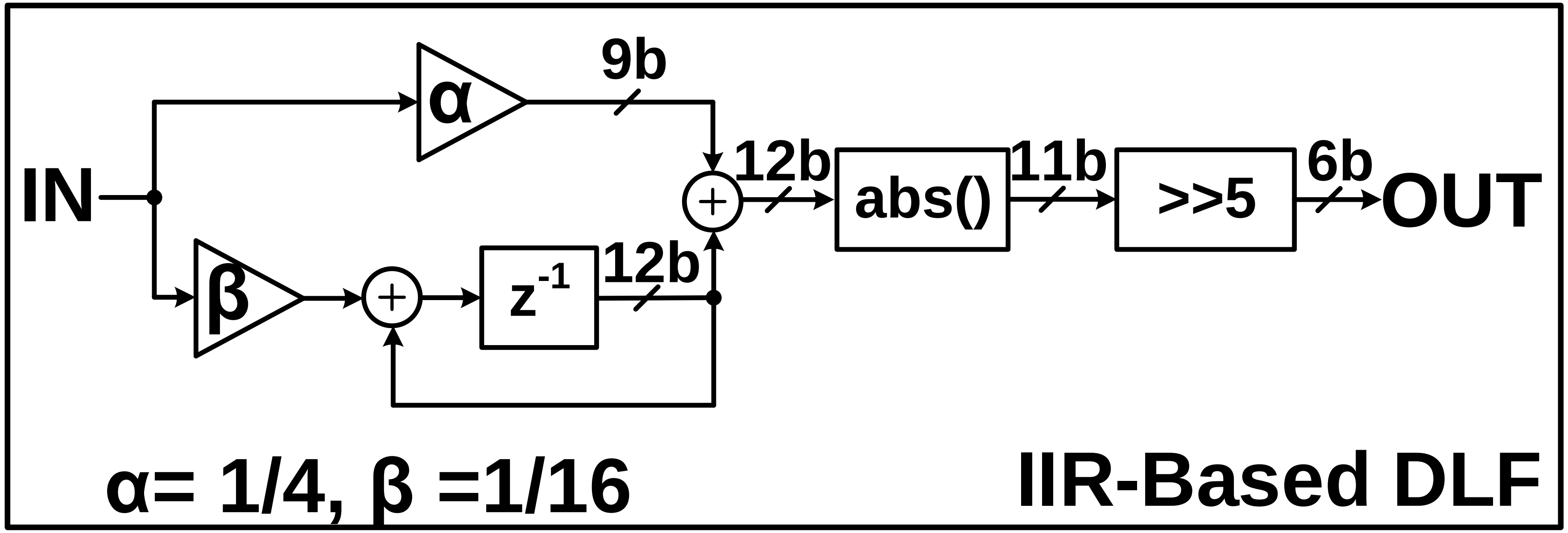
Corners	Loop gain	PM (°)
TT	122.8	60.09
FF	128.1	51.87
FS	125.7	64.16
SF	120.7	54.96
SS	118	64.7

TC & Gm-C Integrator



- ~8 μA under 0.9 V Supply

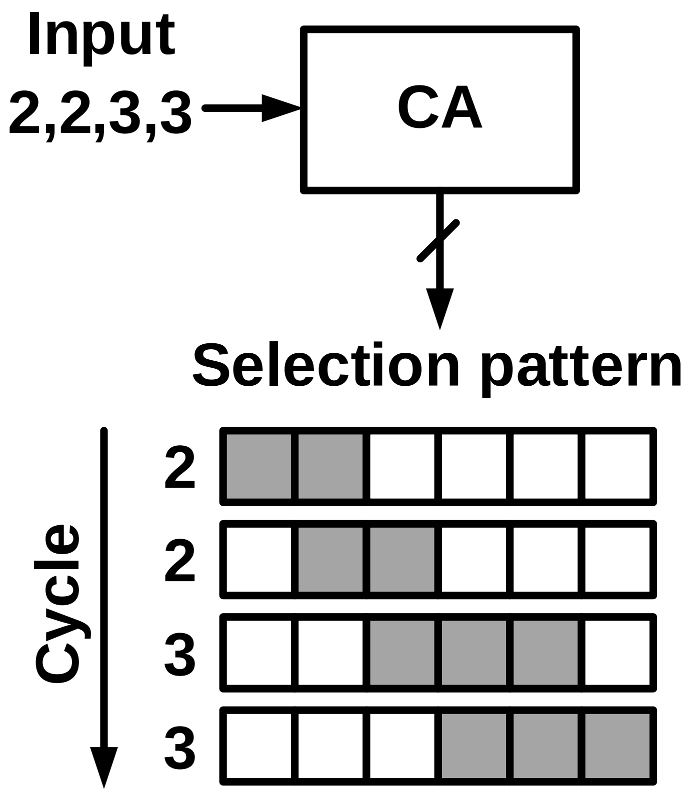
Digital Loop Filter



$$\mathbf{H_{DLF}(z)} = \frac{\boldsymbol{\alpha} + \boldsymbol{\beta} - \boldsymbol{\alpha}\mathbf{z^{-1}}}{\mathbf{1} - \mathbf{z^{-1}}}$$

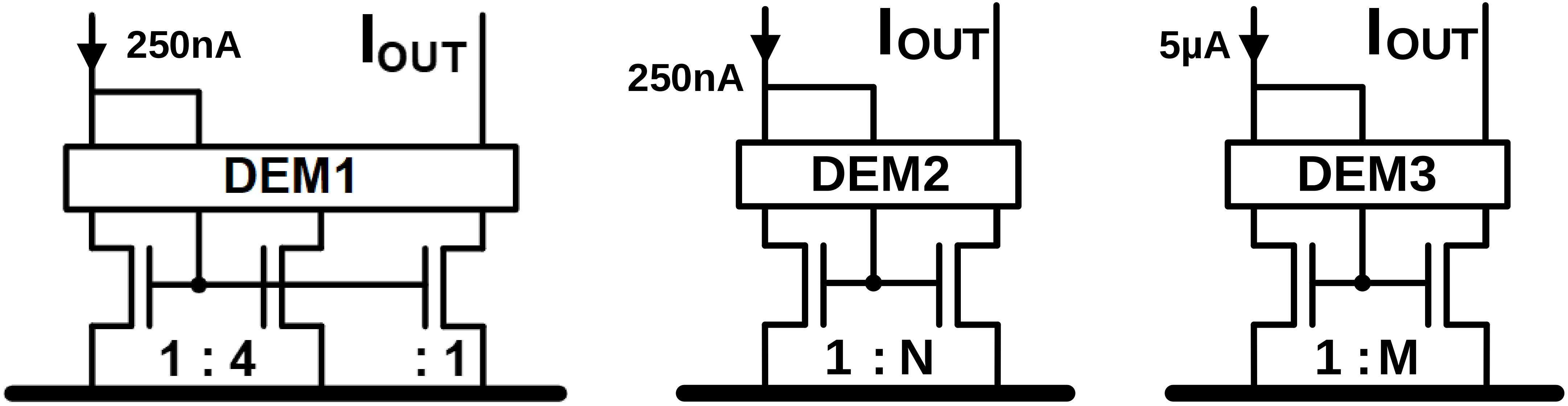
- **매우 큰 DC gain으로 I_{res} 최소화 → input-dependent noise modulation 최소화**

Clock-Averaging (CA) DEM



- **Element 사이의 mismatch를 줄이기 위한 기술.**
- ***1/f* 잡음 완화를 위해 사용될 수 있음.**

DEM Scheme Overview



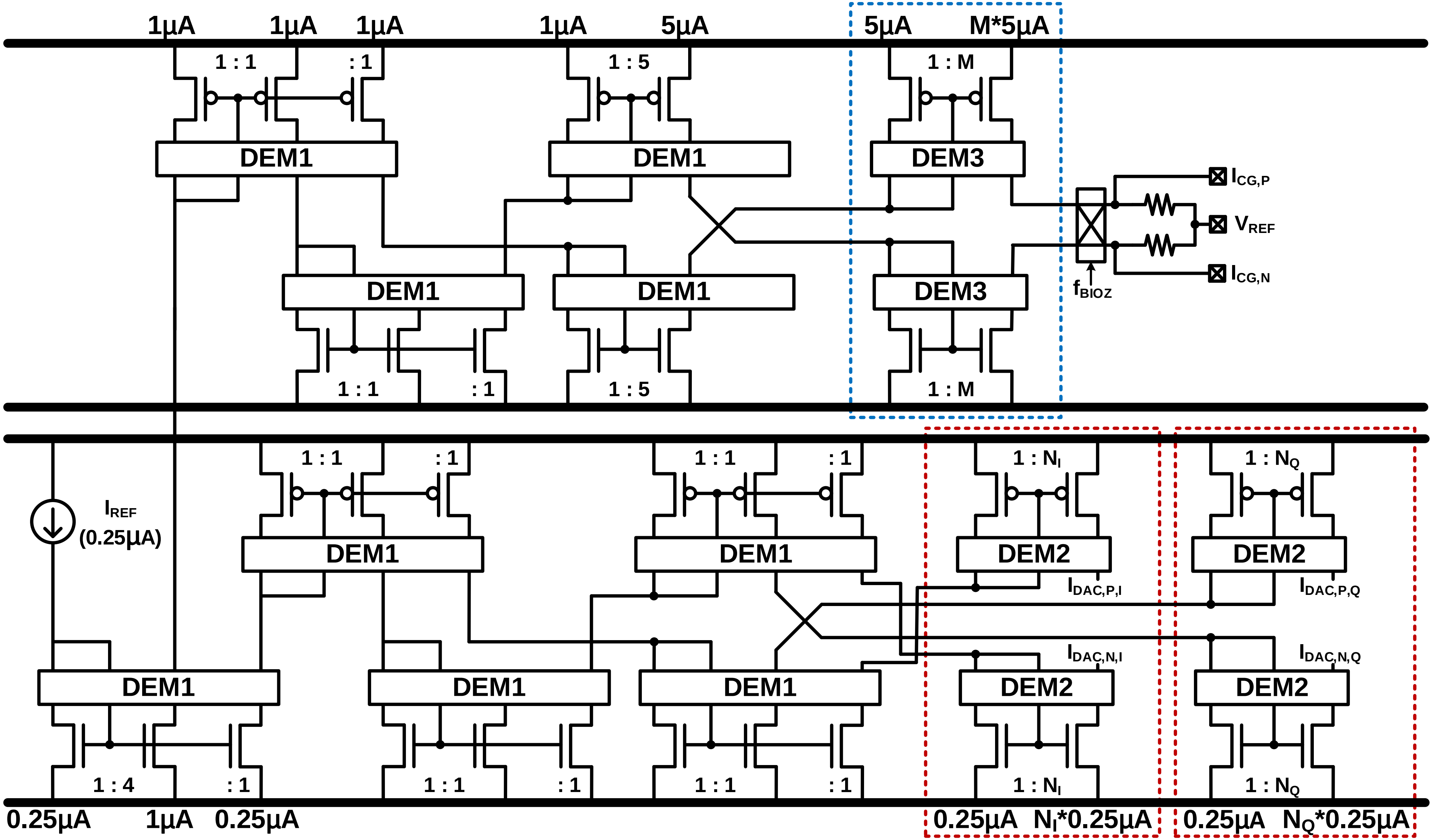
DEM1 for IREF

DEM2 for IDAC

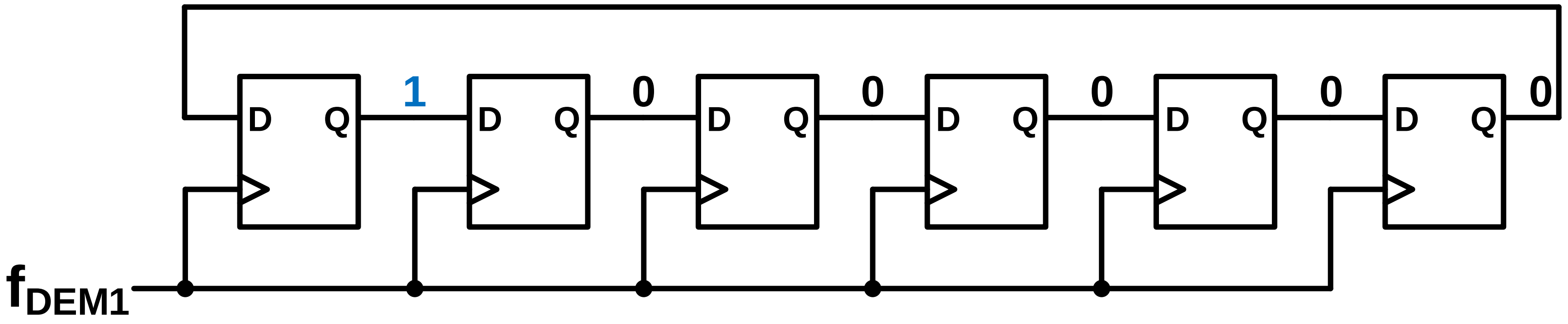
DEM3 for CG

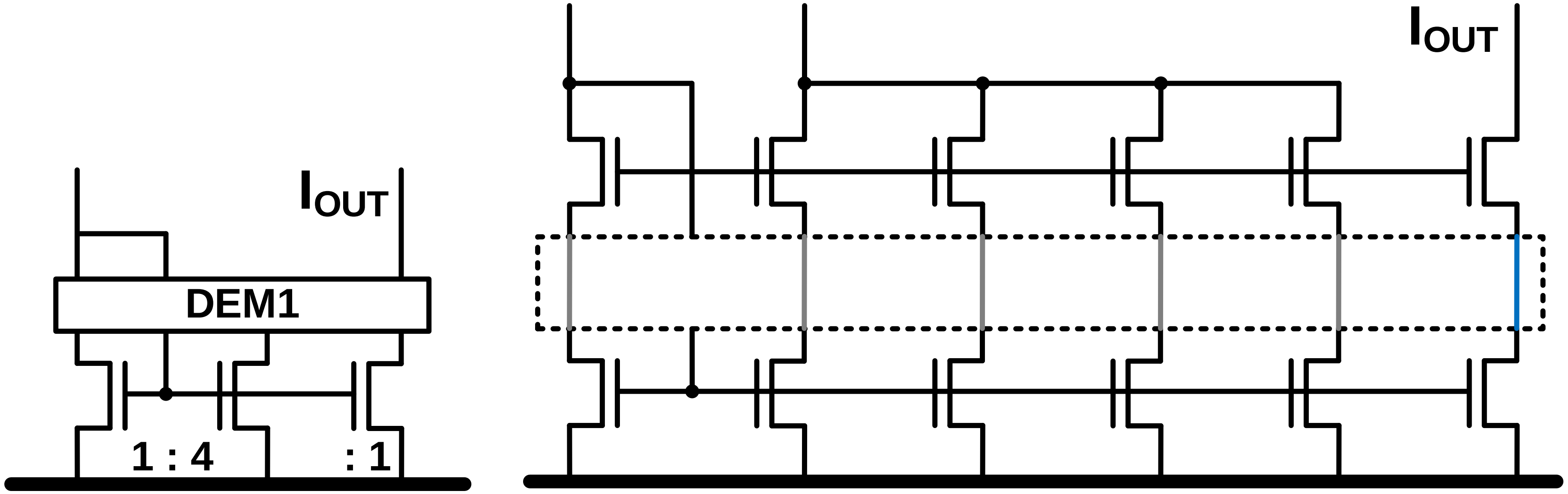
- **1/f 잡음 완화를 위해 Dedicated DEMs 사용.**

DEM Scheme Overview



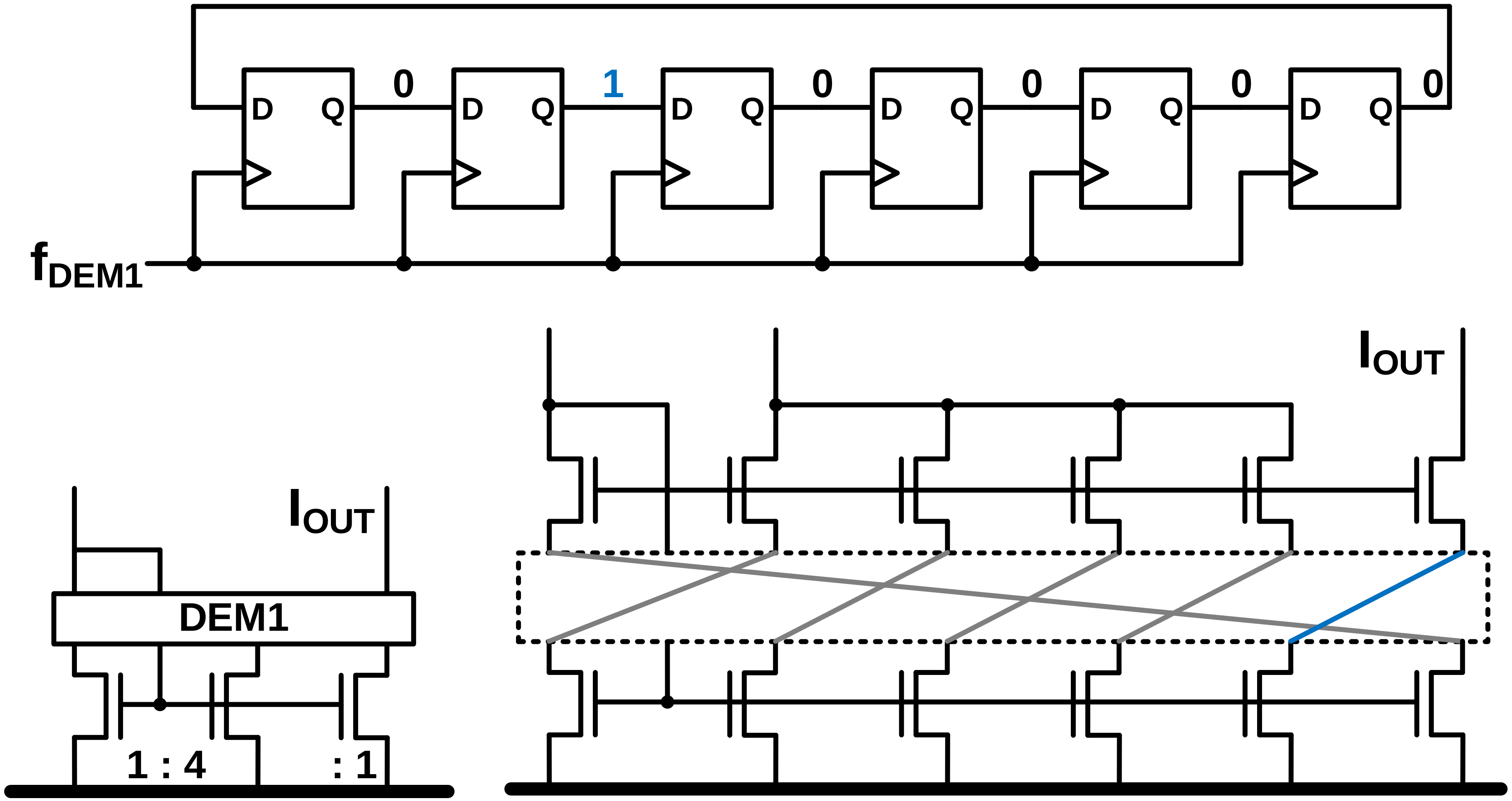
DEM1-IREF





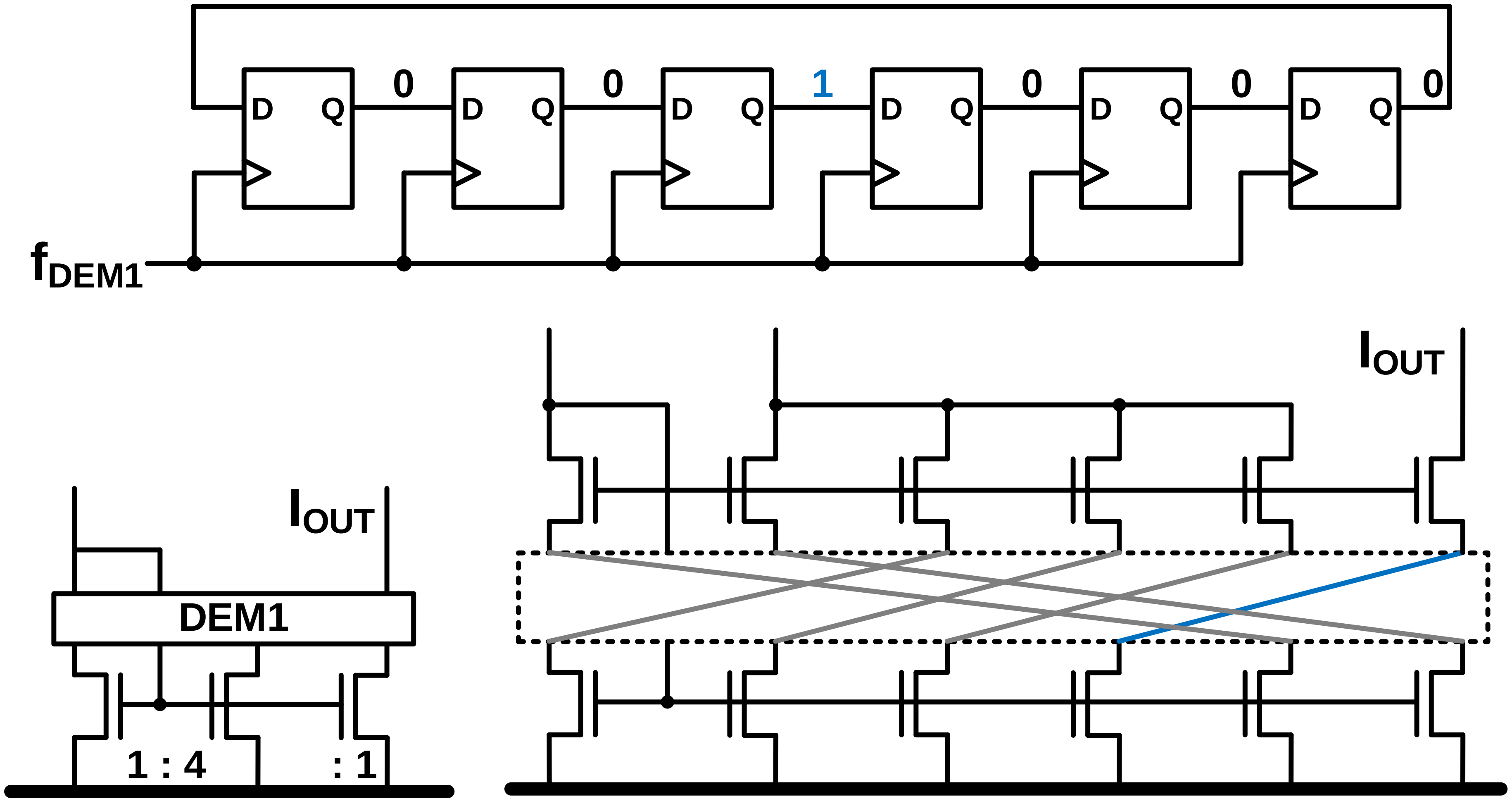
- IREF의 *1/f* noise를 줄이기 위한 DEM1

DEM1-IREF



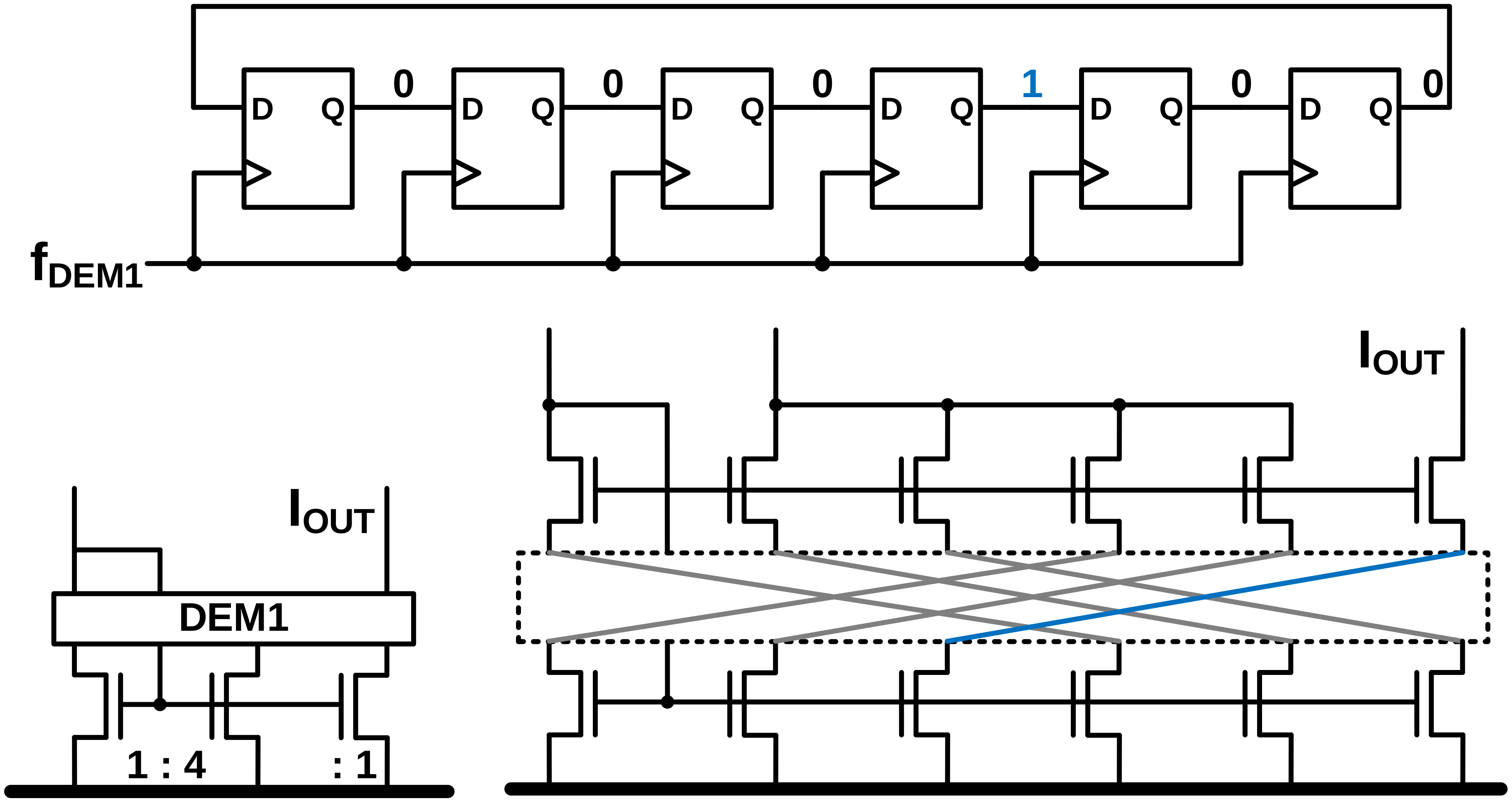
- IREF의 *1/f* noise를 줄이기 위한 DEM1

DEM1-IREF



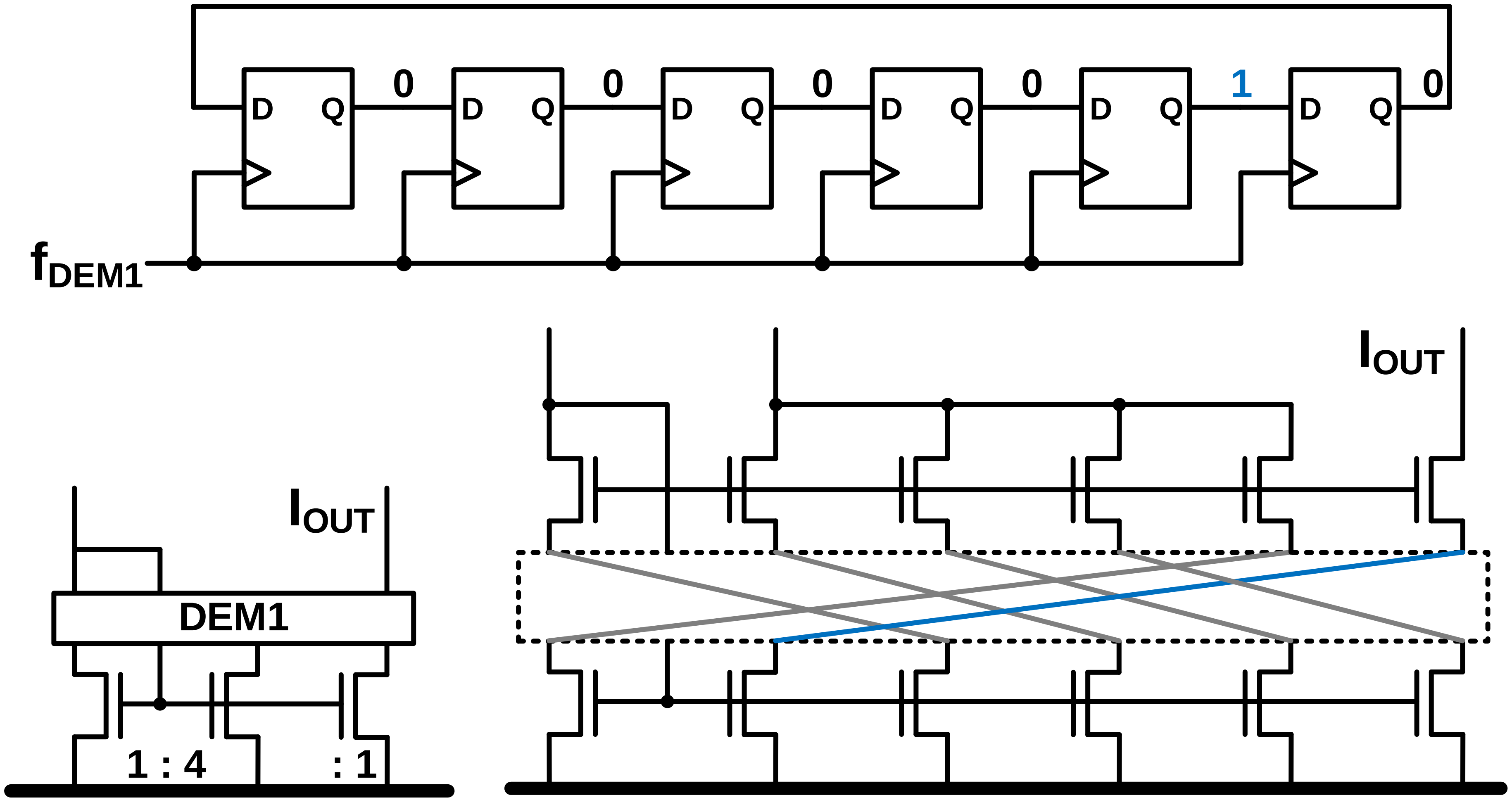
- IREF의 *1/f* noise를 줄이기 위한 DEM1

DEM1-IREF



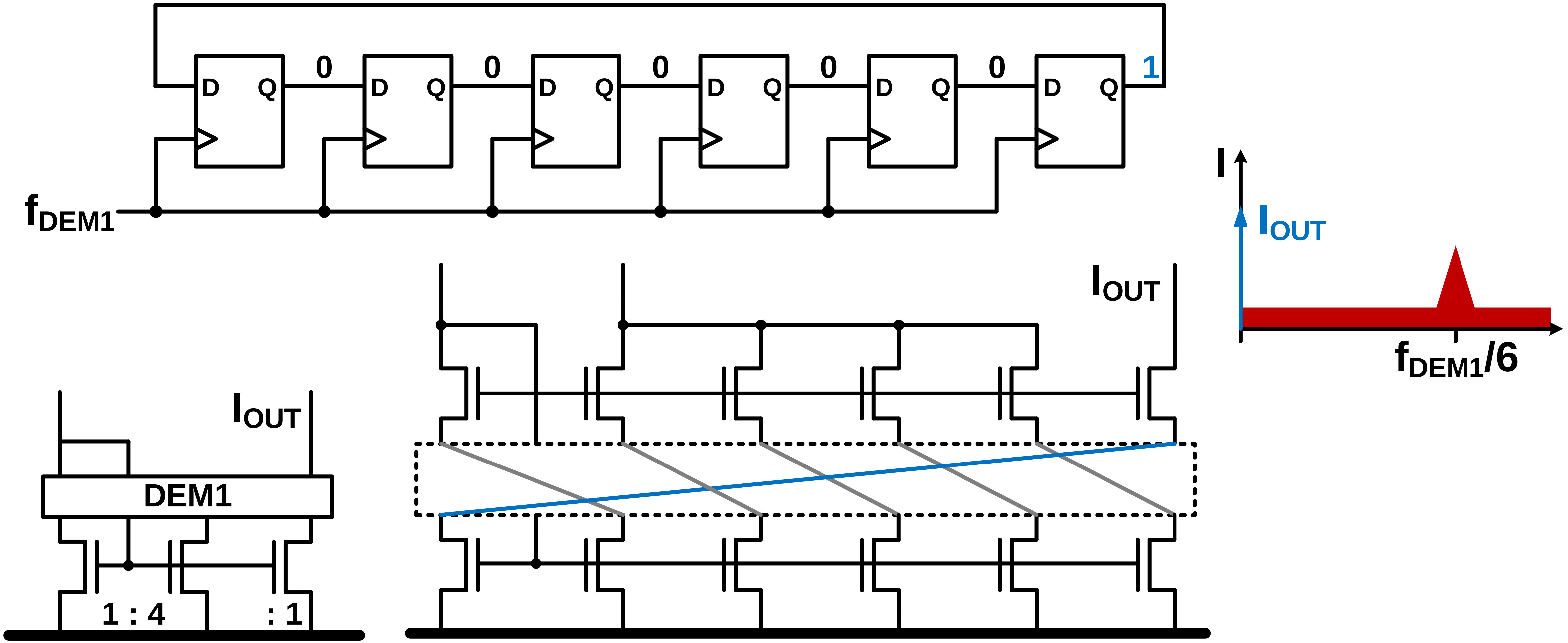
- IREF의 *1/f* noise를 줄이기 위한 DEM1

DEM1-IREF



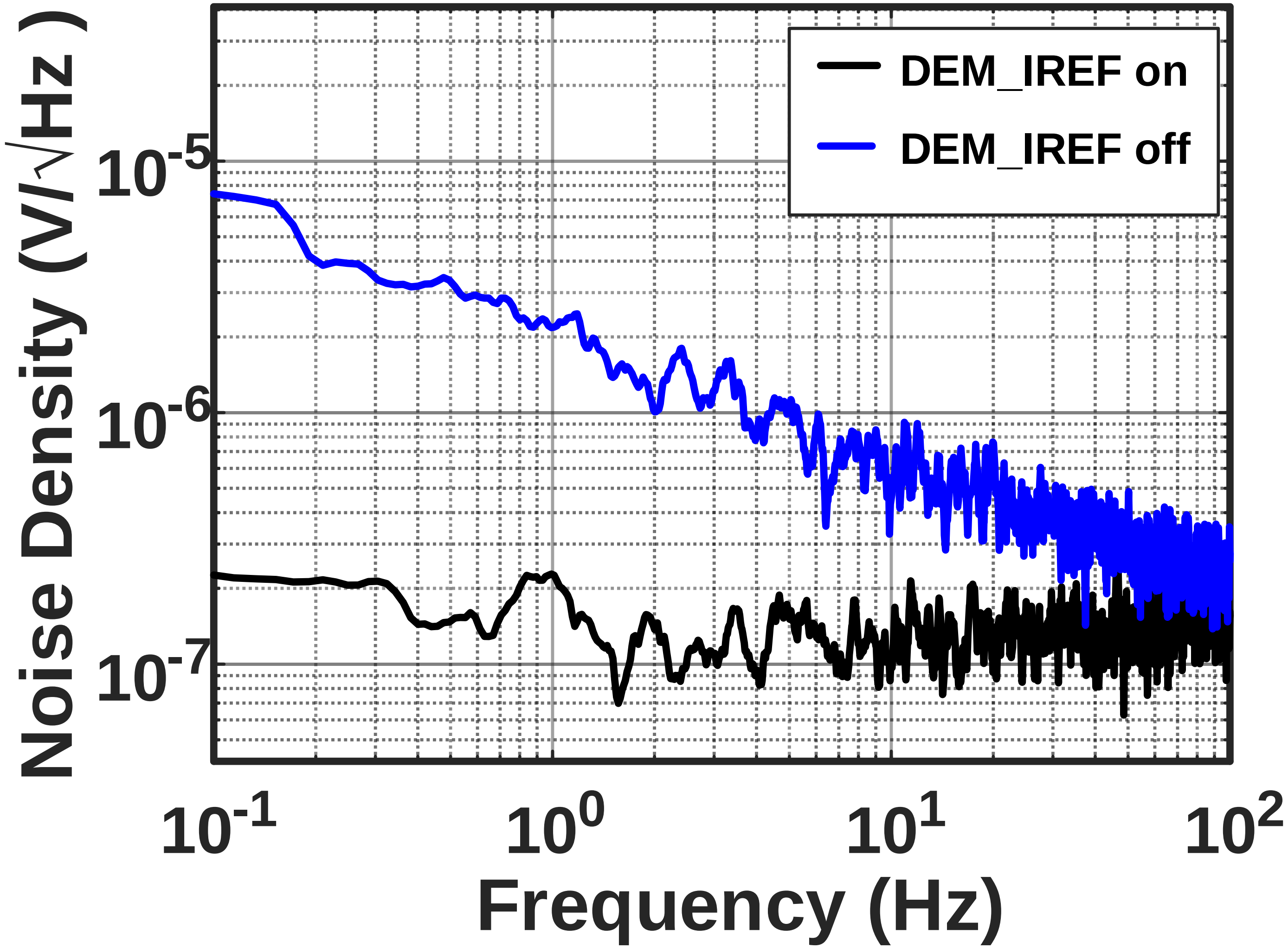
- IREF의 *1/f* noise를 줄이기 위한 DEM1

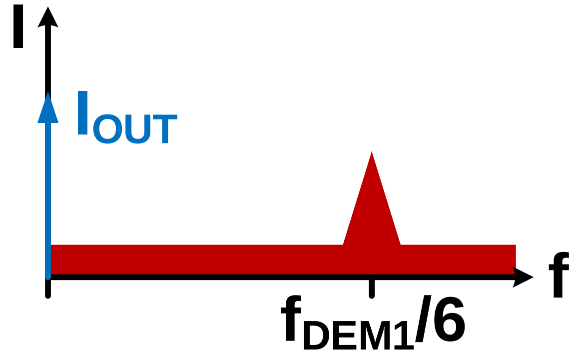
DEM1-IREF



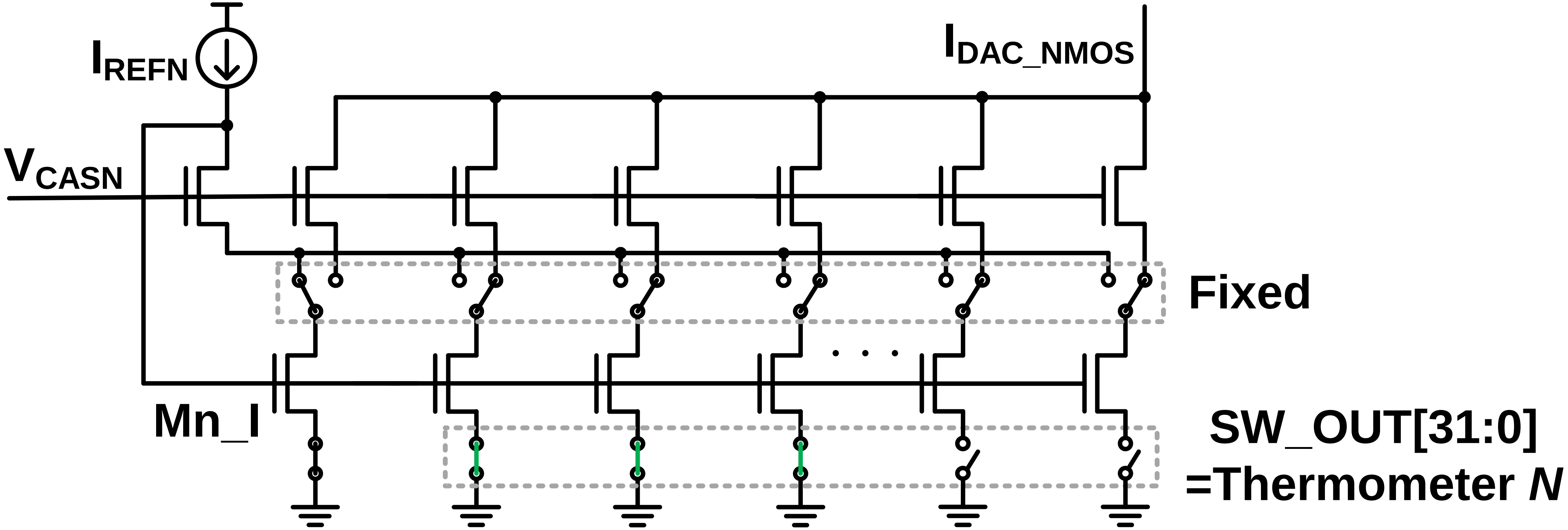
- IREF의 *1/f* noise를 줄이기 위한 DEM1

DEM1 for IREF noise mitigation



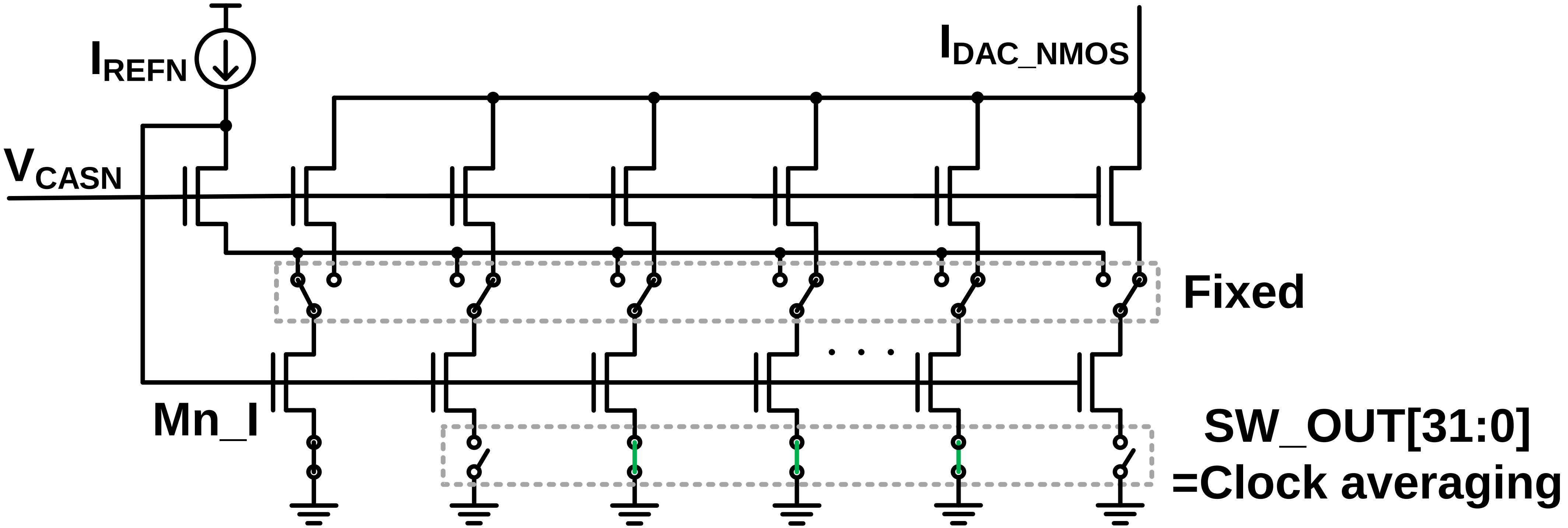


DEM2-IDAC



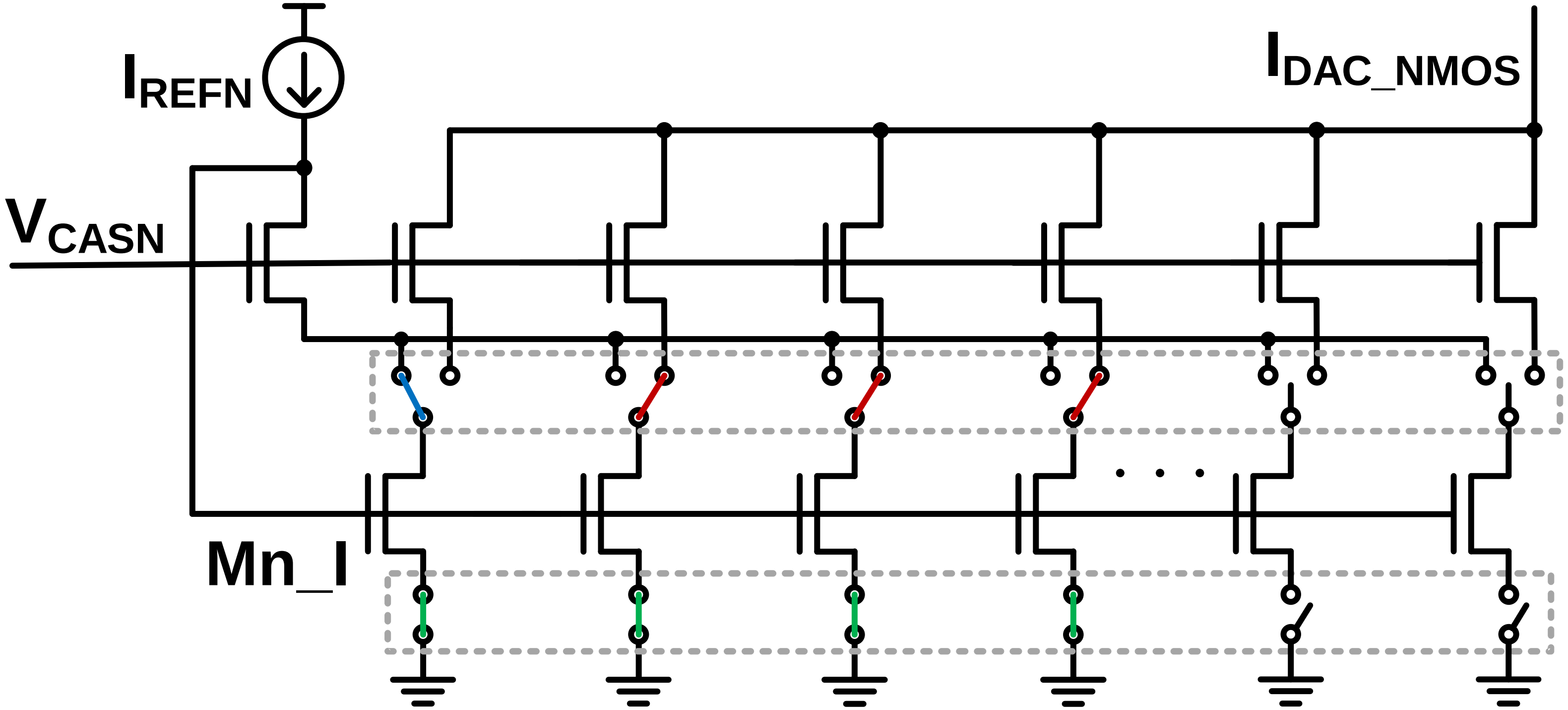
OFF DEM2

DEM2-IDAC



Mn_I & cascode transistors 를 제외하고 ON DEM2

DEM2-IDAC

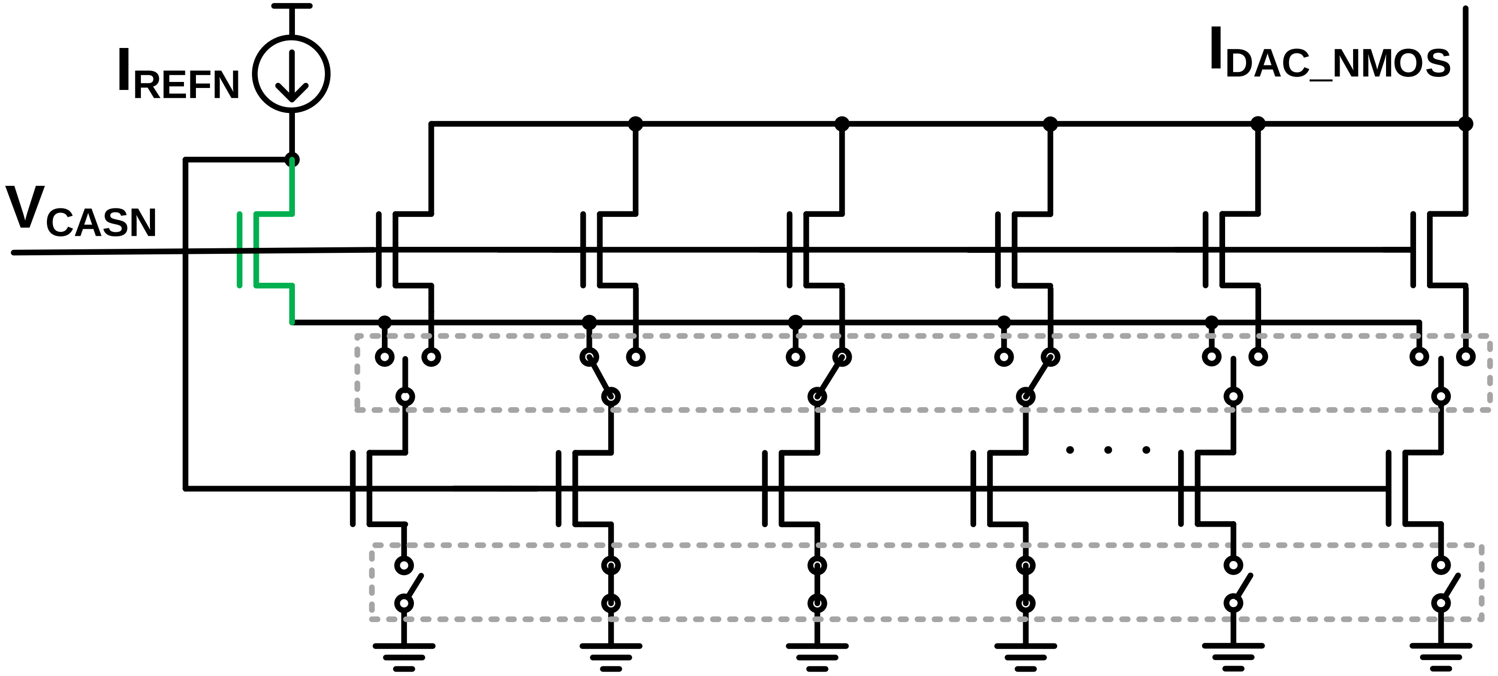


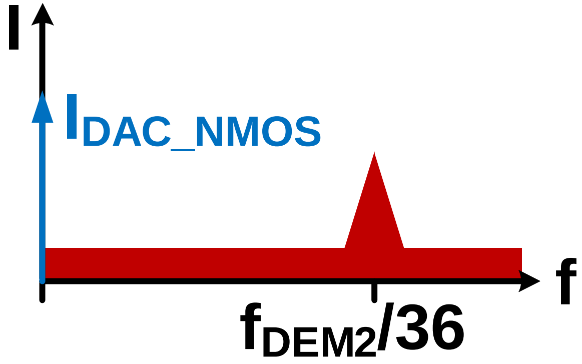
SW1,SW2[32:0]
=Clock averaging w/ M_{CAS}

SW_OUT[32:0]
=Clock averaging w/ Mn_I

Mn_I & cascode transistors 포함하여 ON DEM2

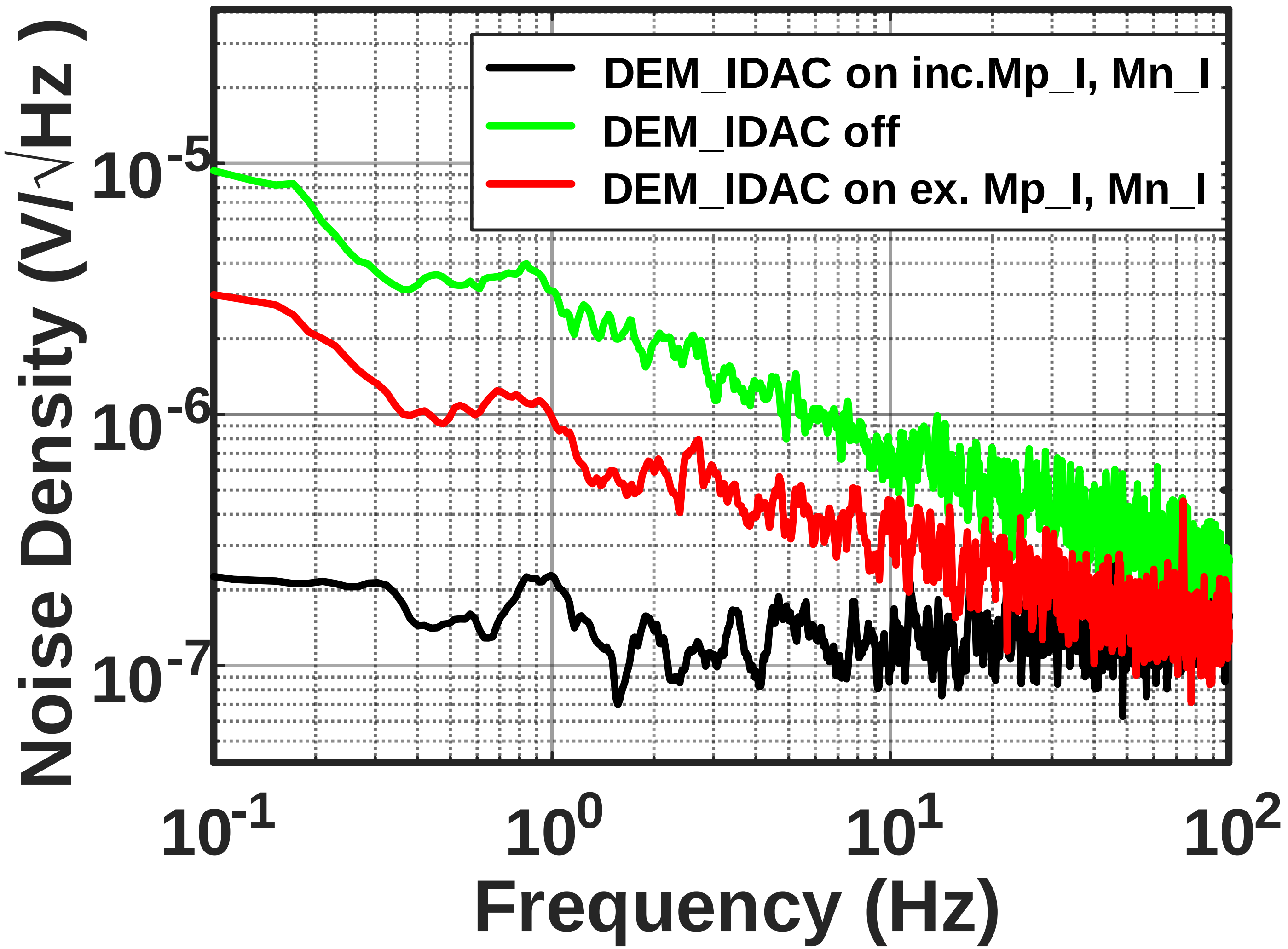
DEM2-IDAC

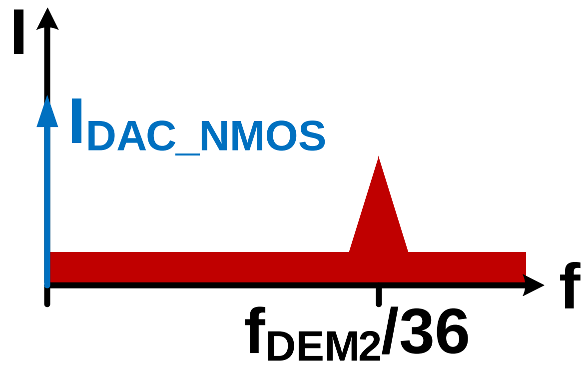




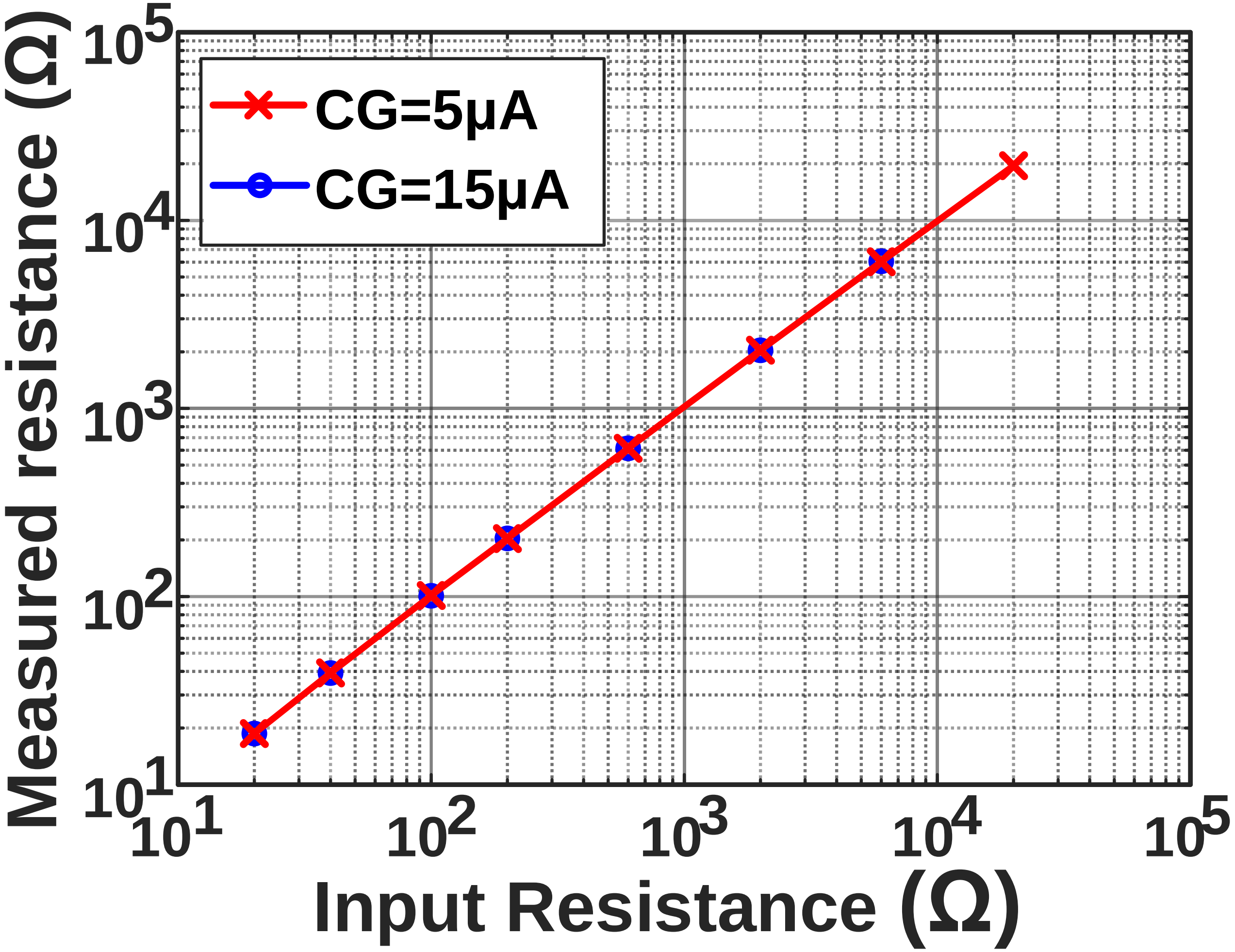
- cascode NMOS (green) 를 제외한 모든 1/f noise가 modulation.
- 총 35 elements (32+1+2 dummy) 구성.

DEM2 for IDAC noise mitigation



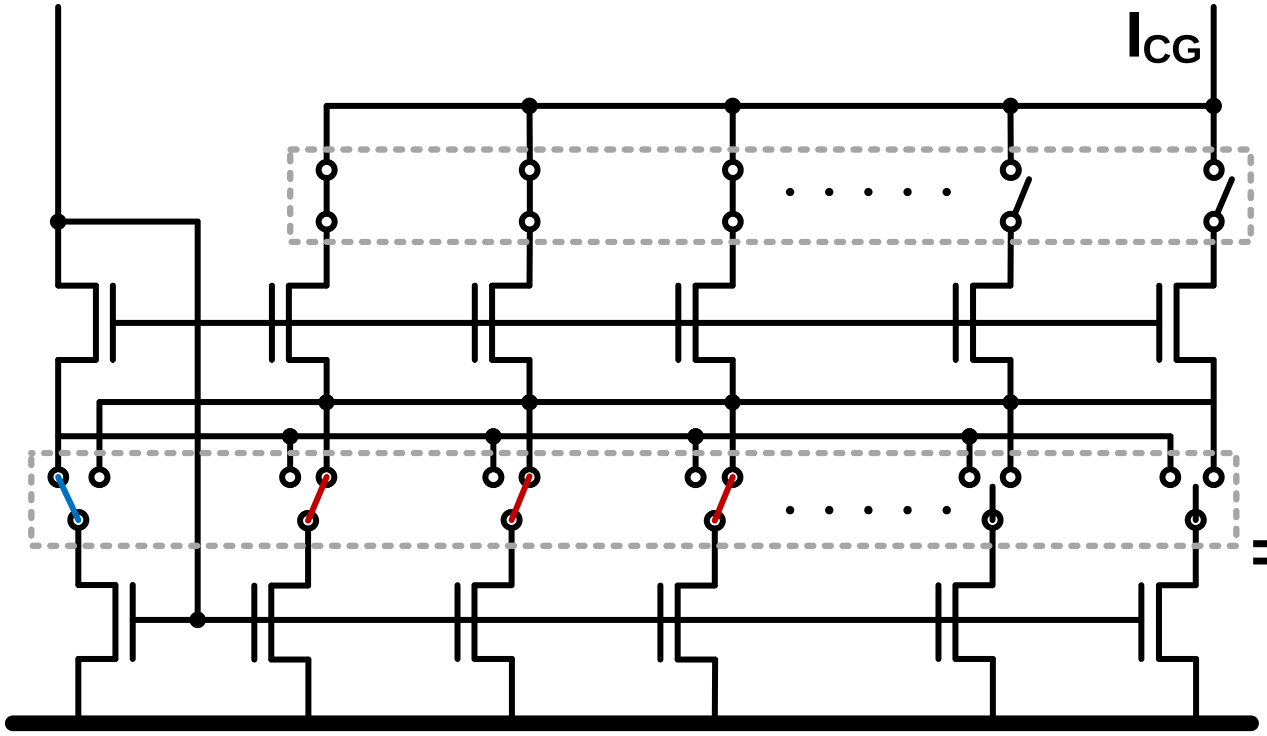


Linearity Measurement



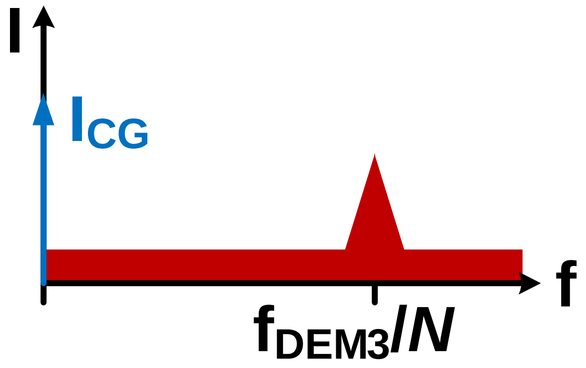
- R^2= 0.999919 @ CG=5 μA. R^2= 0.999988 @ CG=15 μA.

DEM3-CG



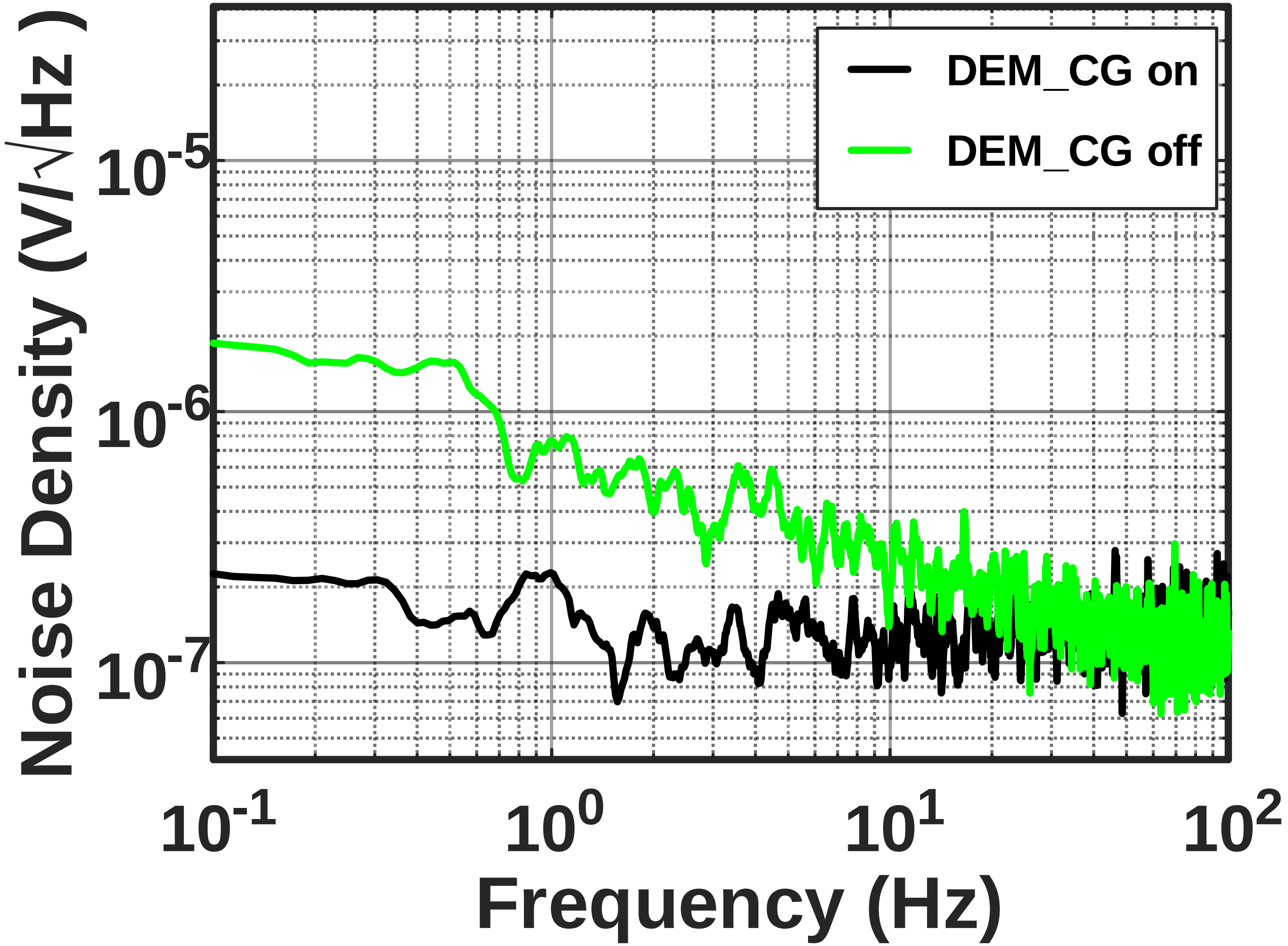
SW_OUT[19:0]
=thermometer *N*

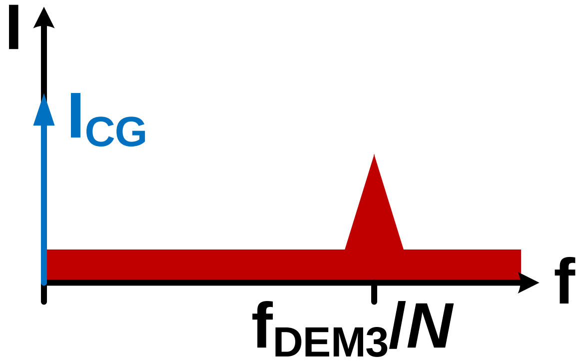
SW_CS[20:0]
=Clock averaging



- I_{CG} 의 출력 전류 크기 (*N*) 가 modulation frequency 결정.

DEM3 for CG noise reduction

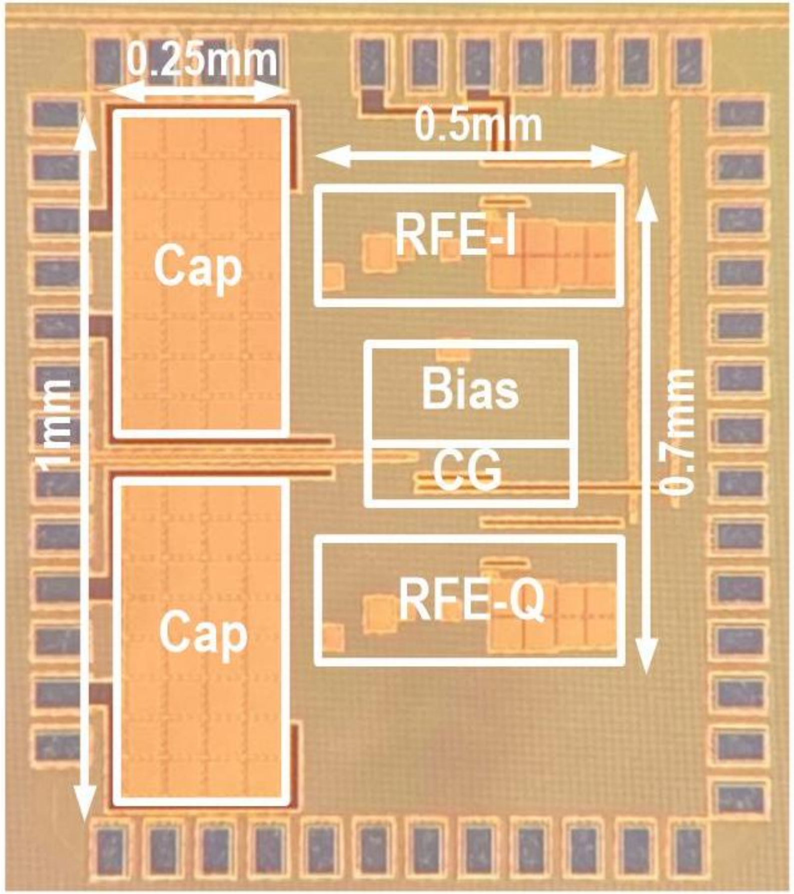




Outline

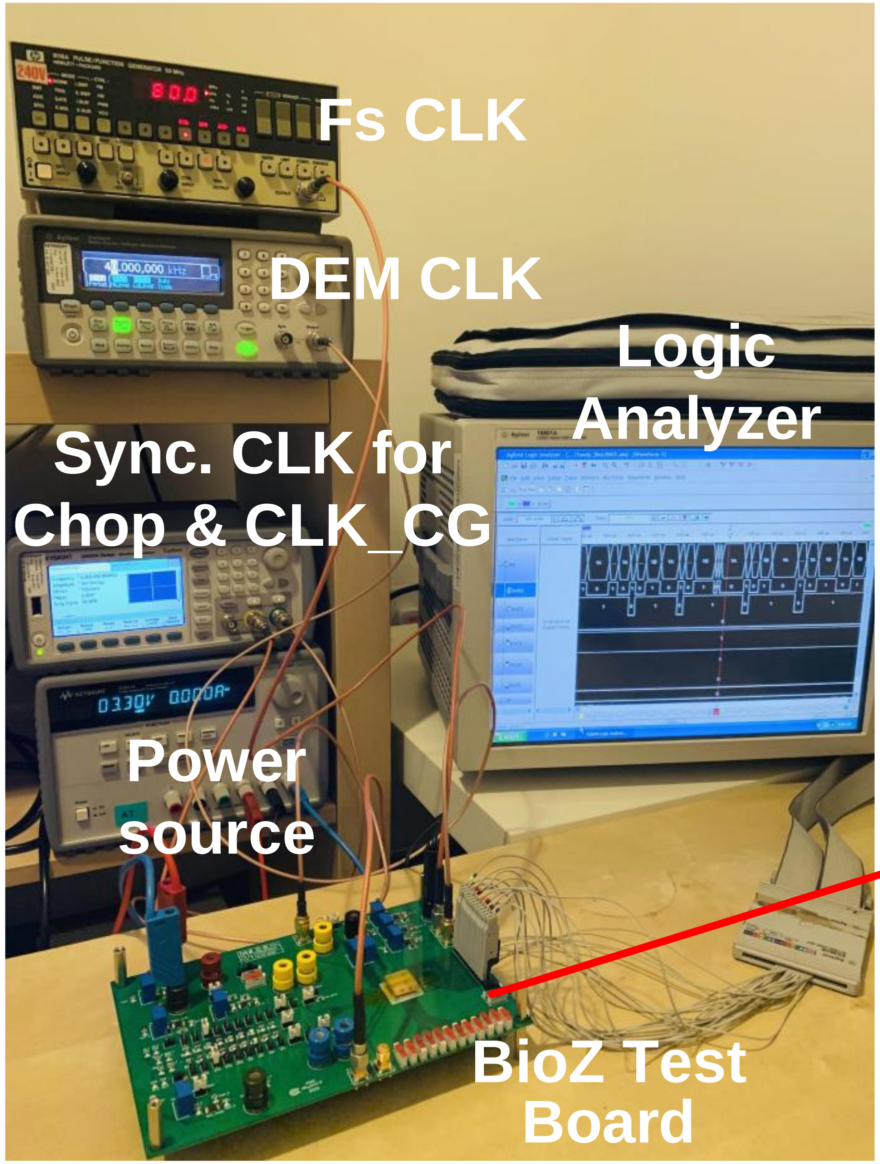
- Motivation
- BioZ Readout Overview
- Proposed BioZ Readout IC
- **Measurement results**
- Conclusions

Chip Photo and Area

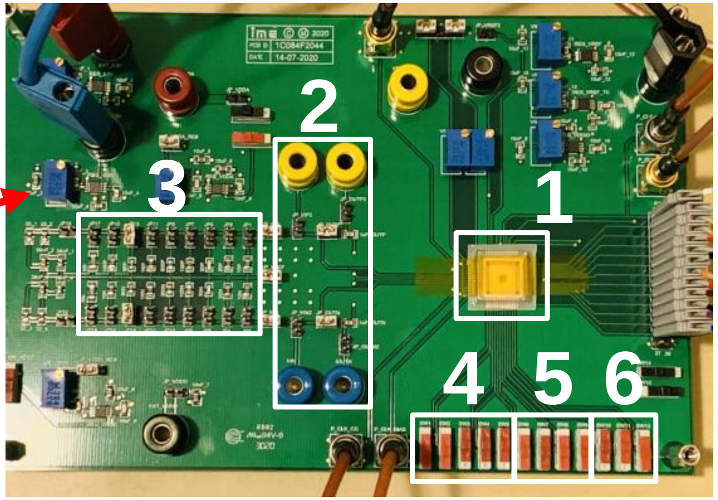


- 40nm CMOS process
- Area: 0.6 mm^2

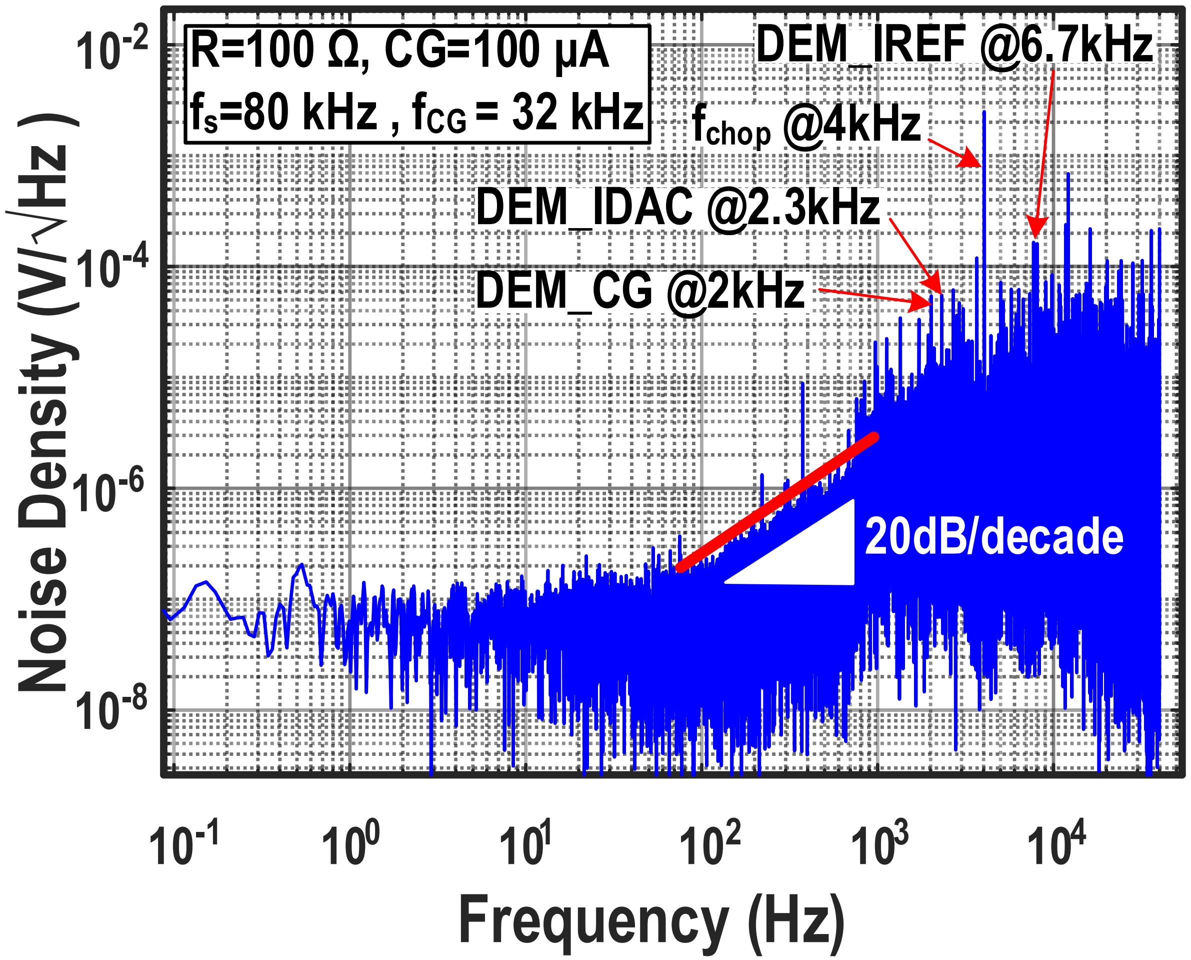
Setup



1. BioZ Readout IC
2. Pins for 2E & 4E test
3. Resistor bank
4. Digital control for CG
5. DEMs control for IREF, CG, IDAC
6. Control of DLF coefficients

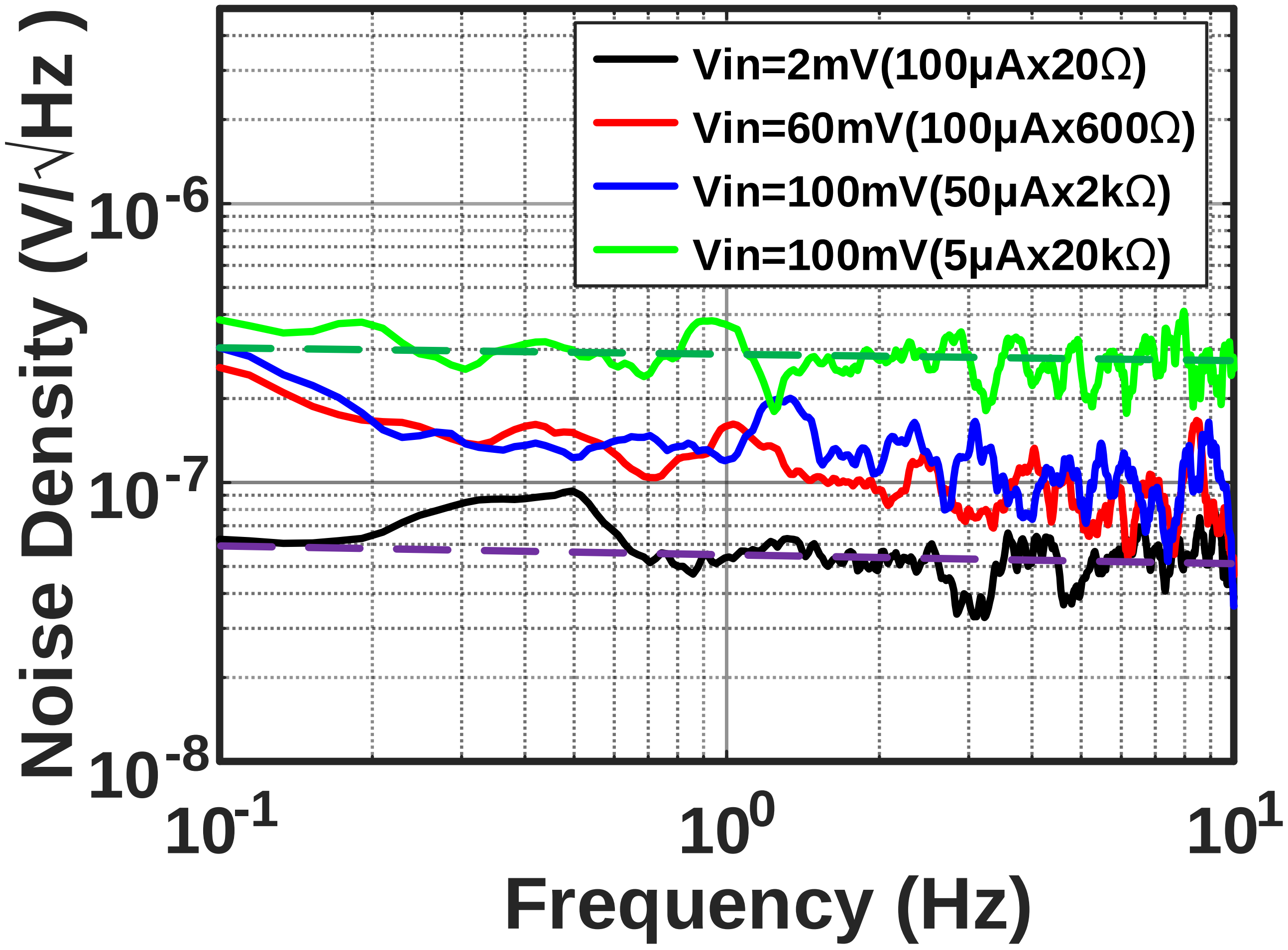


Noise Spectrum



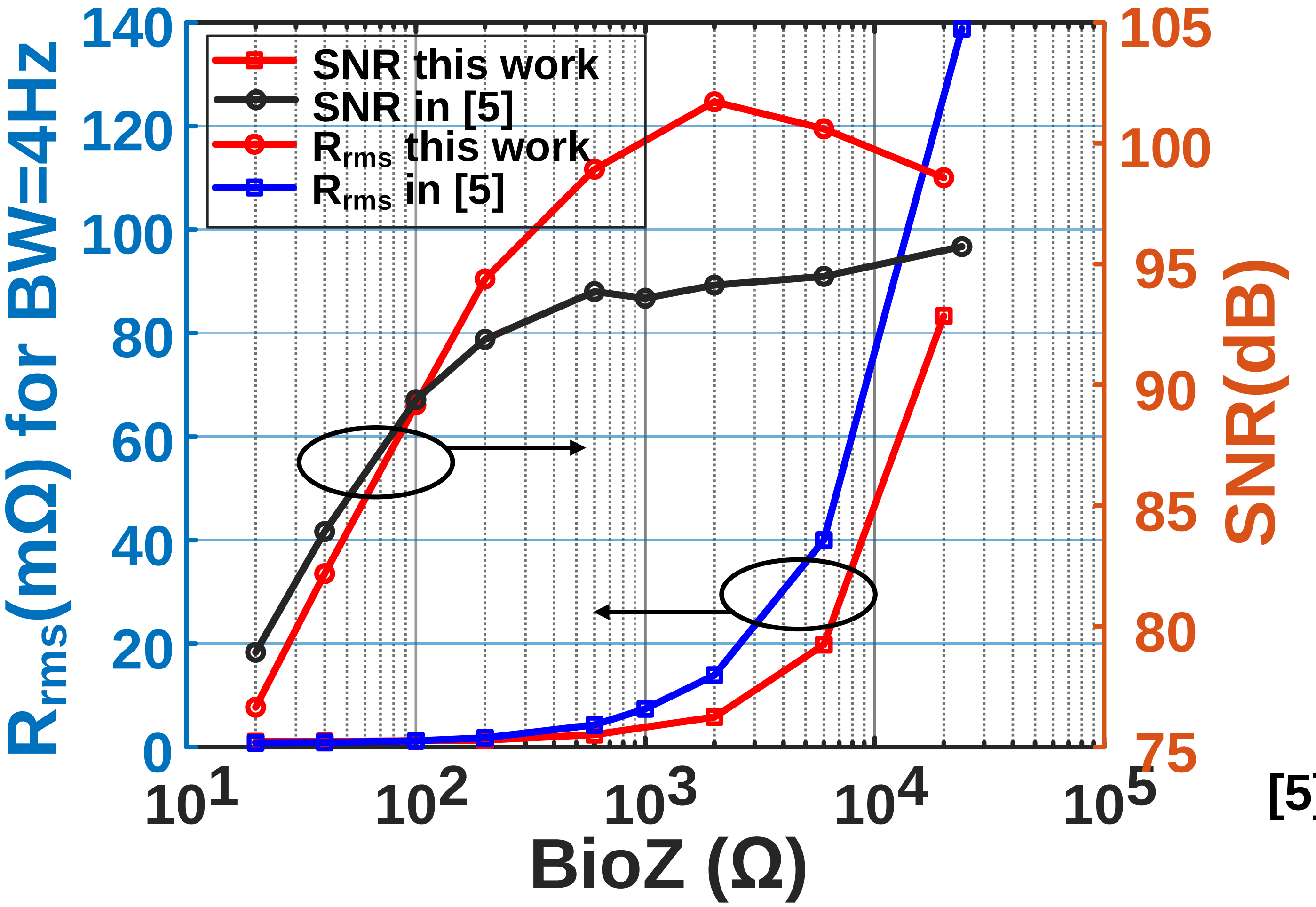
- <0.1 Hz 1/f noise corner & 1차 noise shaping

Noise Measurement



R_{in} (Ω)	Noise Density @ 1 Hz [mΩ/√Hz]	RMS noise (0.1- 4 Hz) [$m\Omega_{rms}$]	SNR (dB)
20	0.52	1.04	76.6
40	0.54	1.08	82.3
100	0.62	1.23	89.2
200	0.68	1.35	94.4
600	1.28	2.4	98.9
2k	2.91	5.8	101.7
6k	9.94	19.8	100.6
20k	41.8	83.3	98.6

Noise & SNR

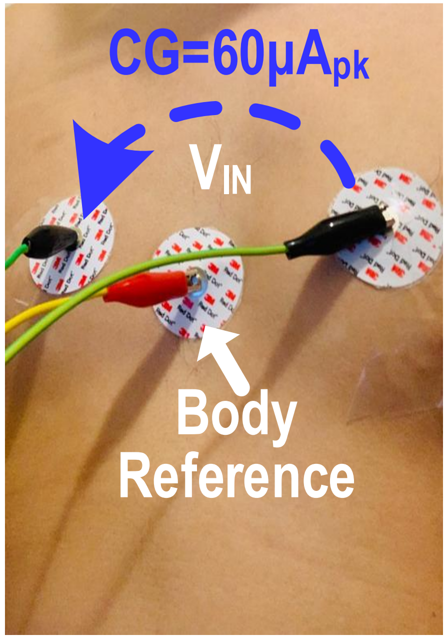


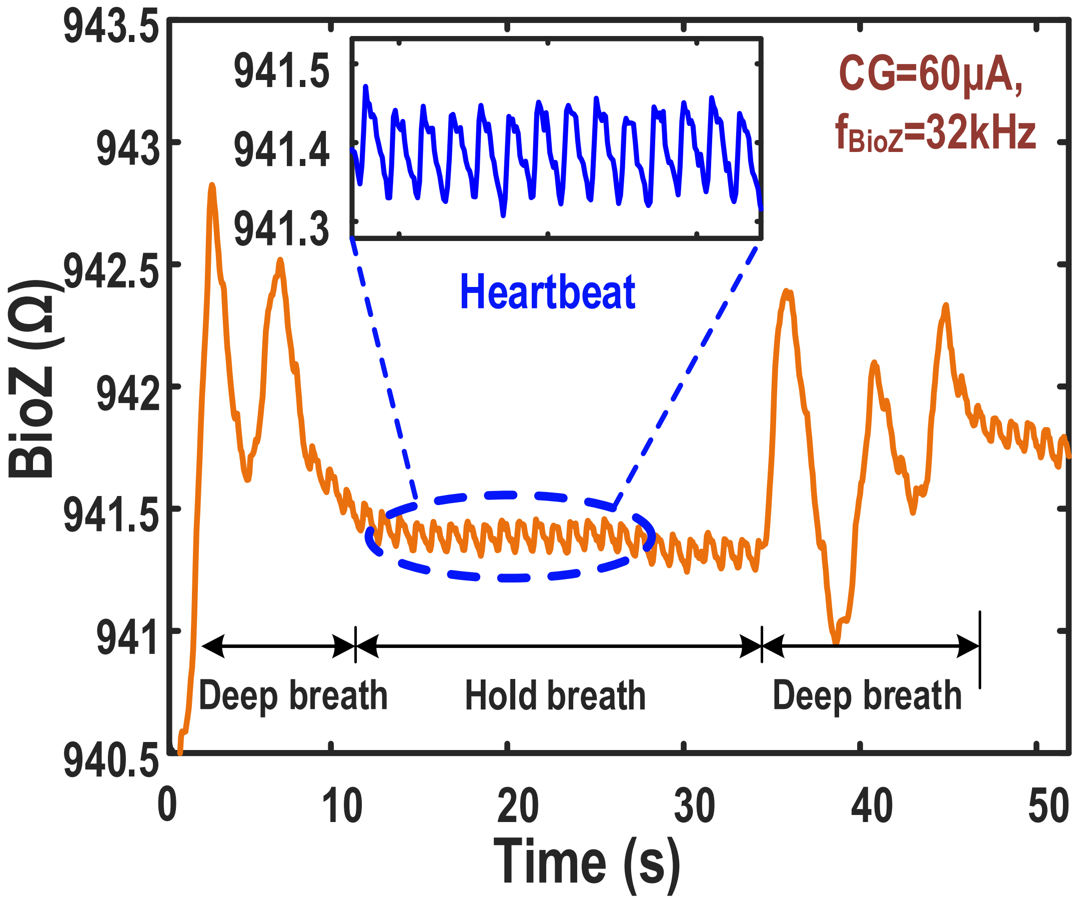
[5] H. Ha, ISSCC 2019

- Max. SNR=101.9 dB

In-vivo Measurement (2E)

2-Electrode Setup

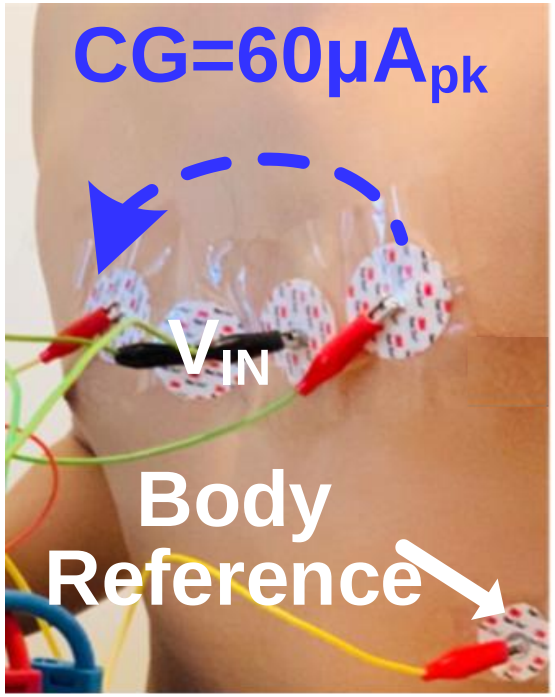


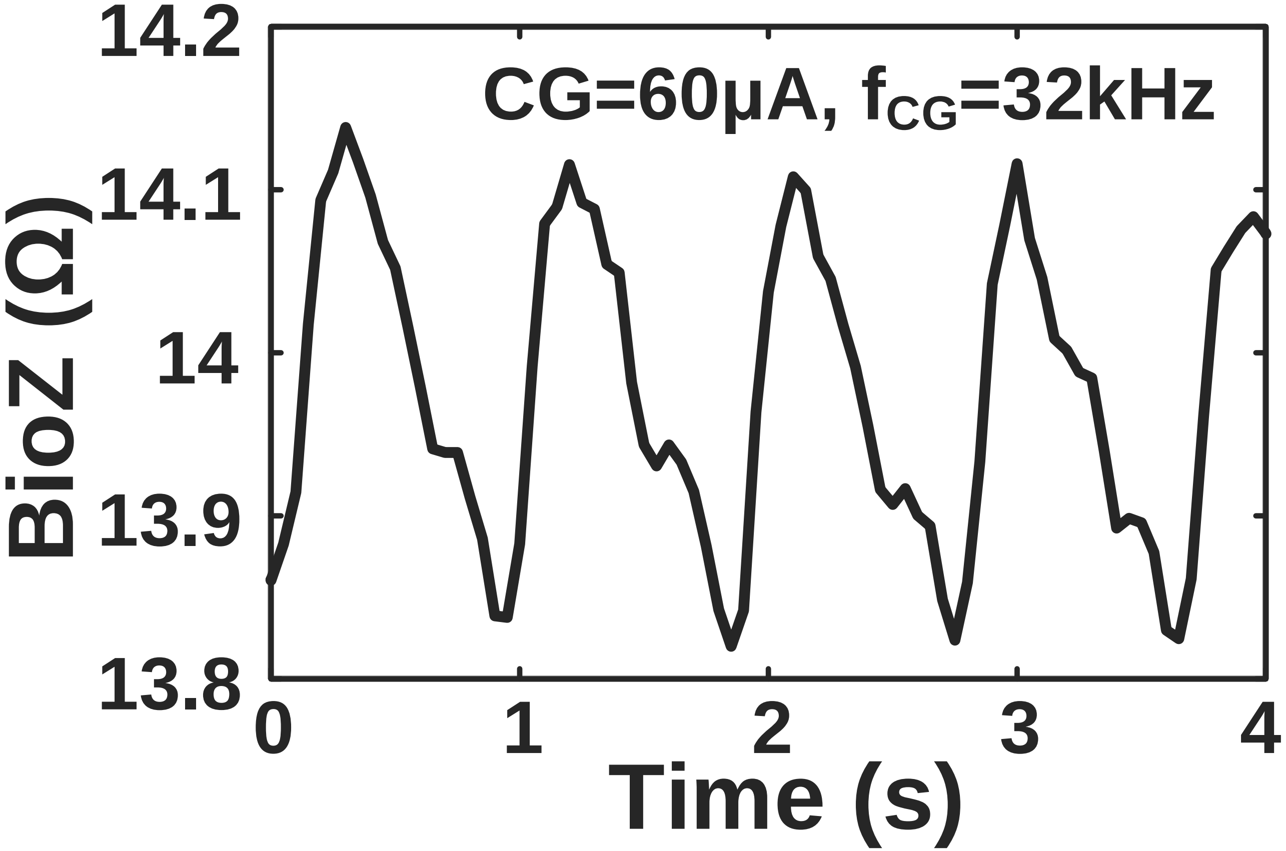


- 가슴에 2 전극 setup을 통한 호흡 신호 관찰

In-vivo Measurement (4E)

4-Electrode Setup





- 가슴에 4 전극을 통한 심장 박동 관찰.

Benchmark Table

Parameters	VLSI'17 [2]	JSSC'18 [3]	JSSC'19 [5]	MAX30001	ADS1292R	This work
Tech. (μm)	0.18	0.13	0.055	N/A	N/A	**0.04**
Supply (V)	1.2/1.8	1.5/3.5	1.2	N/A	N/A	**0.9/0.6**
Stimulation signal	Square (I)	Pseudo-sine (I)	Square (I)	Square (I)	Square (V)	**Square (I)**
Input range (kΩ)	1	10	24	5.625	10	**20**
Current magintude (μA_{pk})	5~100	5~50	5~100	8~96	0~100	**5~100**
Current frequency (kHz)	1~1024	4~100	1~1024	0.125~131	32~64	**1-1024**
Noise Density Rn @ 1Hz (mΩ/sqrt(Hz))	1.1 (R=20Ω) 26 (R=1kΩ)	0.7 (R<50Ω) 9.5 (R=2kΩ)	0.4 (R=40Ω,100μA_{pk}) 7 (R=2kΩ,60μA_{pk})	40[a] (R=680Ω)	40[a] (R=2kΩ)	**0.52 (R=20Ω,100μA_{pk}) 2.9 (R=2kΩ,50μA_{pk})**
SNR_{max}(dB)[b] (BW=4 Hz)	76.6	91.4	95.7	78.6	87.9	**101.9**
Power (μW) of Readout	18.7	89[d]	18.9 ~34.9	N/A	N/A	**8.8~16**
Power (μW) of CG	54~229	56~95	31~154.7	N/A	N/A	**17.8 ~ 103.3**
Power (μW)	72.7~247.7	145~184	49.9~189.6	320	335	**26.6~119.3**
Area (mm^2)	0.88	0.96	0.74	N/A	N/A	**0.6**
FoM (dB)[c]	124.5	135.6	143.5	119.6	128.6	**152.6**

[a] Peak-to-peak value [b] SNRmax=max(R/Rrms) where Rrms=Rn*√BW or Rpp/√2

[c] FoM= SNRmax+10*log(BW/Power) where power is the sum of max. in readout and min. in CG

Conclusion

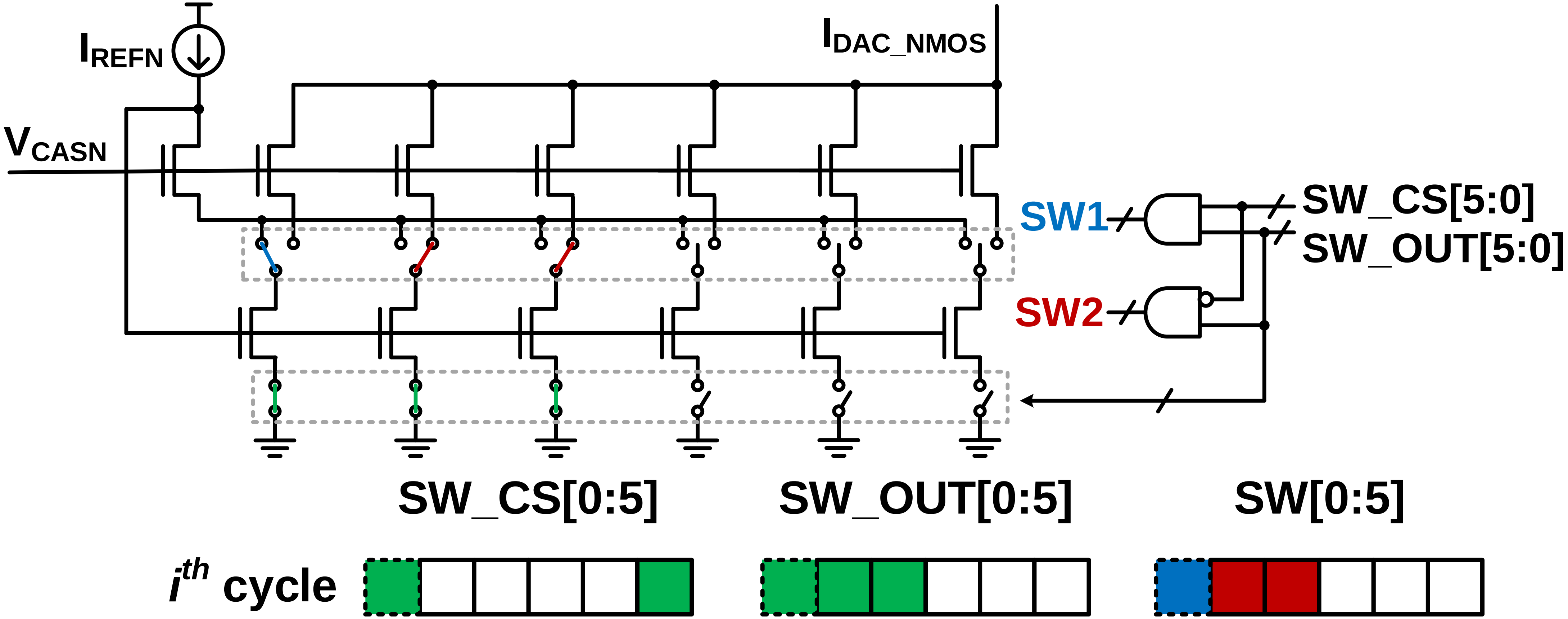
- **2E & 4E setup을 위한 ΔΣ기반의 BioZ 판독회로**
  - 고 해상도를 위한 1차 noise-shaping + DLF
  - 1/f noise 완화를 위한 dedicated DEM schemes 사용

- **state-of-the-art performance 달성**
  - 101.9 dB의 최대 SNR과 20kΩ의 넓은 입력 범위
  - <0.1 Hz 1/f noise corner
  - 0.6V/0.9V 전압에서 8.8−16 μW 전력 소모

- **in-vivo test 통한 시연**

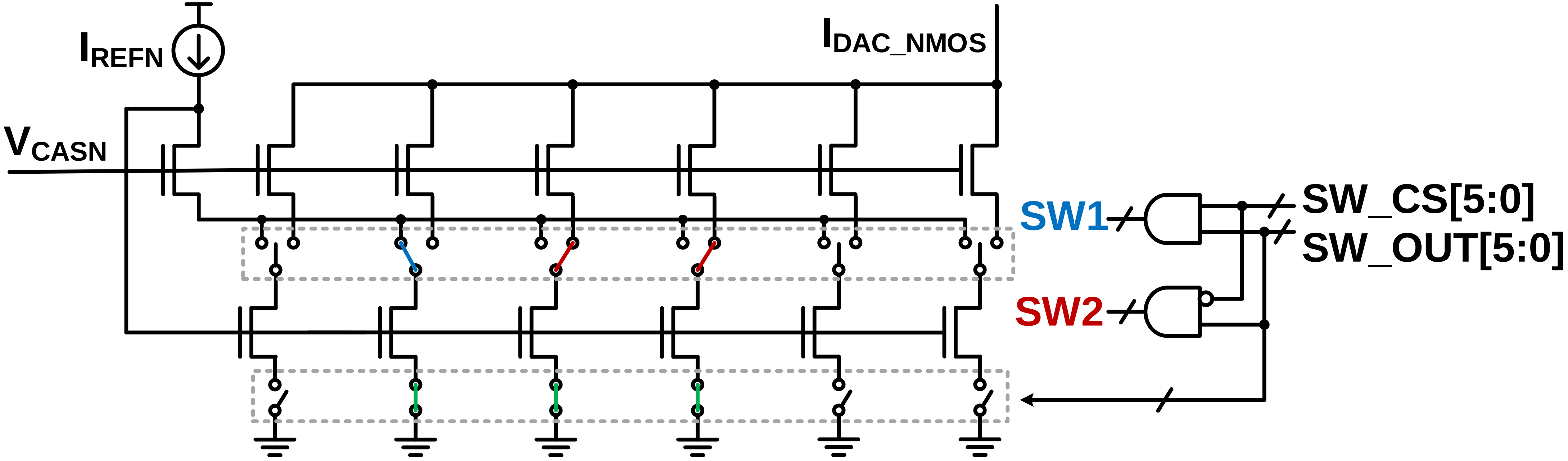
DEM2-IDAC

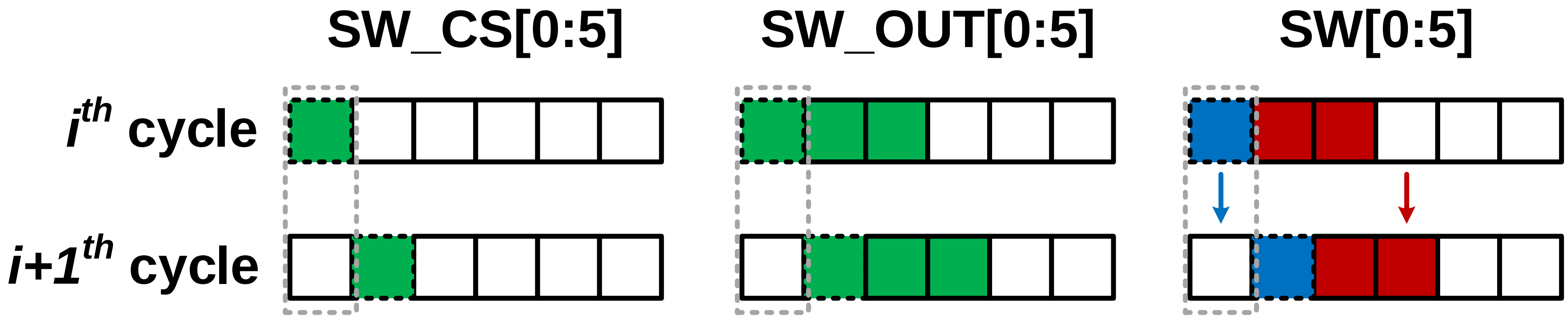
Example: 5 IDACs



DEM2-IDAC

Example: 5 IDACs

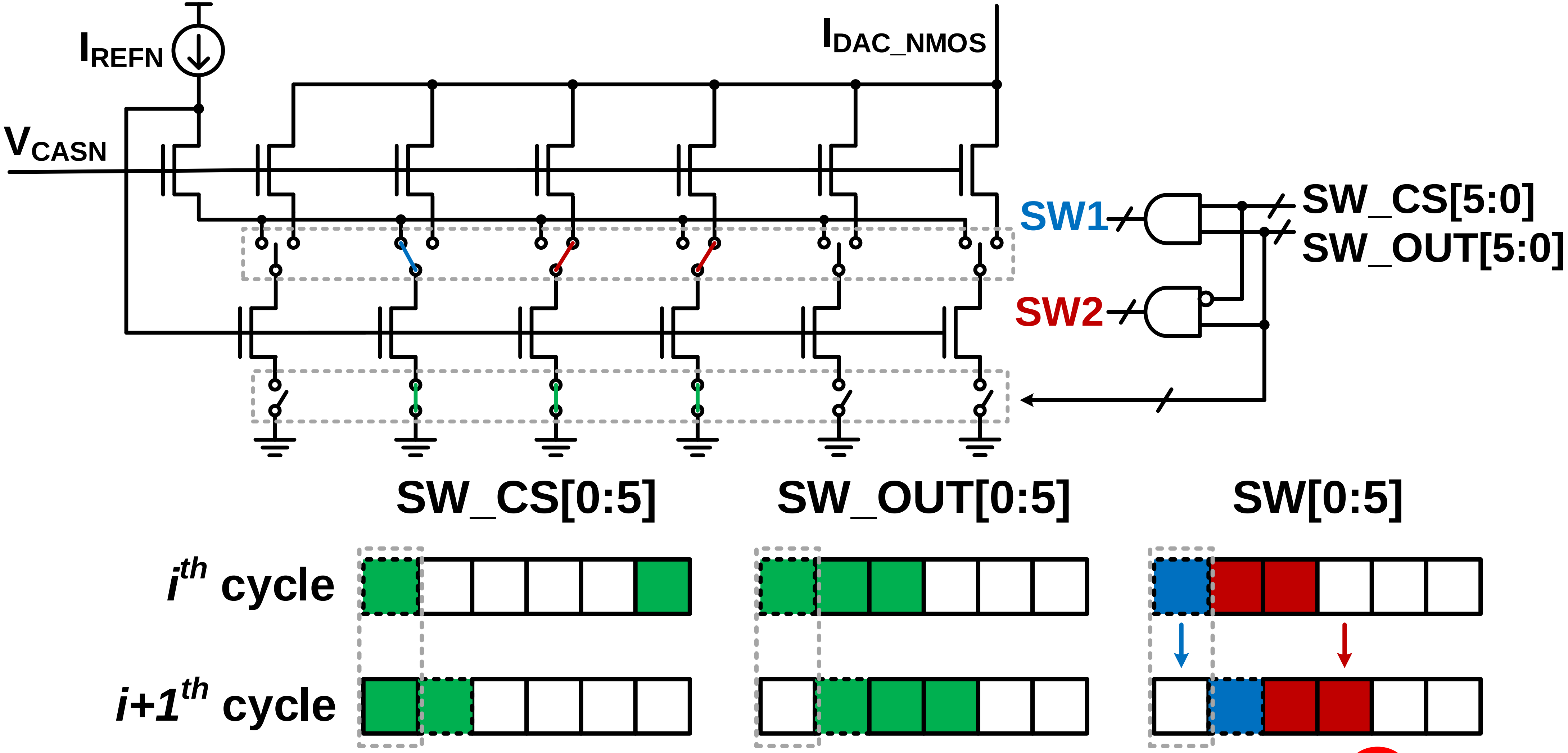




- SW_CS & SW_OUT 두 신호 모두가 current source의 off timing 결정. ☹

DEM2-IDAC

Example: 5 IDACs



- 오직 SW_OUT 신호가 current source의 off timing 결정. ☺