부경대학교 반도체 설계 및 MPW제작 서비스
운영 워크샵(2025-04-04)

My Chip 서비스 기반
아날로그-디지털 컨버터(ADC) 개발

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Jeju National University

Department of Electronic Engineering

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- My Chip 서비스 기반 ADC IP 4종
- 결론 및 향 후 계획

연구실 소개

➢Jeju Mixed-signal IC Lab. [JMICL] (2023~)

- **Over GS/s ADC&DAC** for wired & wireless communication systems

참여 인력

연구책임자: 오동렬

- ✓Analog & Digital ICs
- ✓Giga S/s 1-Ch. ADC using flash, SAR, pipeline
- ✓Tens of Giga S/s Time-interleaved ADC
- ✓Digital calibration for channel mismatches

석사과정 (8명)

*: My Chip 참여


이재강(*)


김범진(*)


김한준(*)

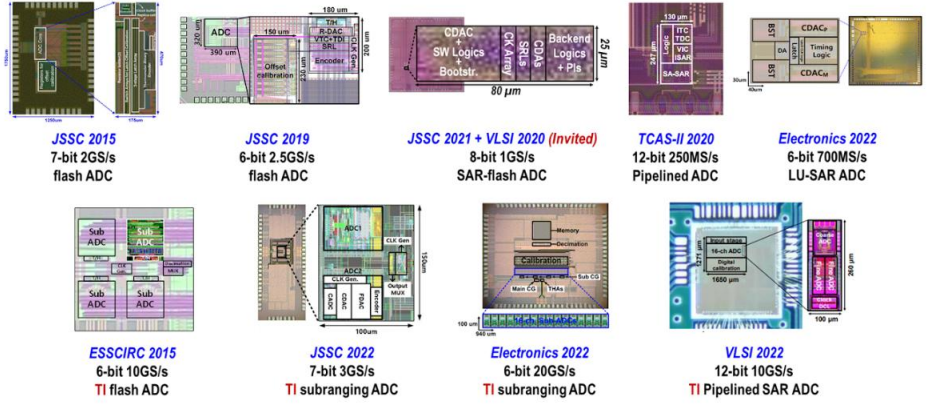

오상원(*)

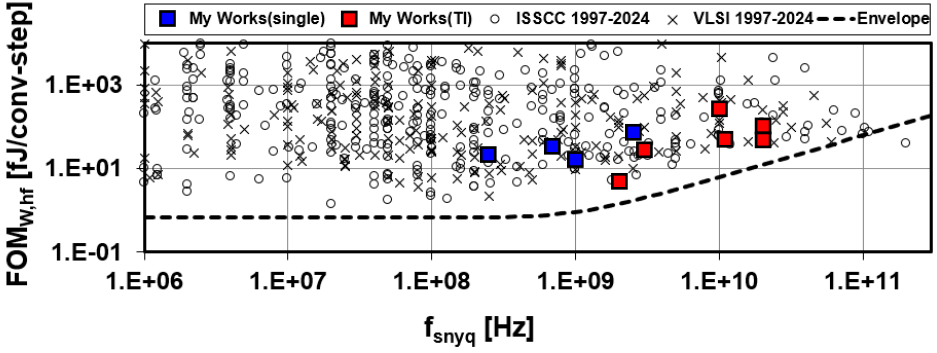

김다연(*)


황현기(*)


윤예원

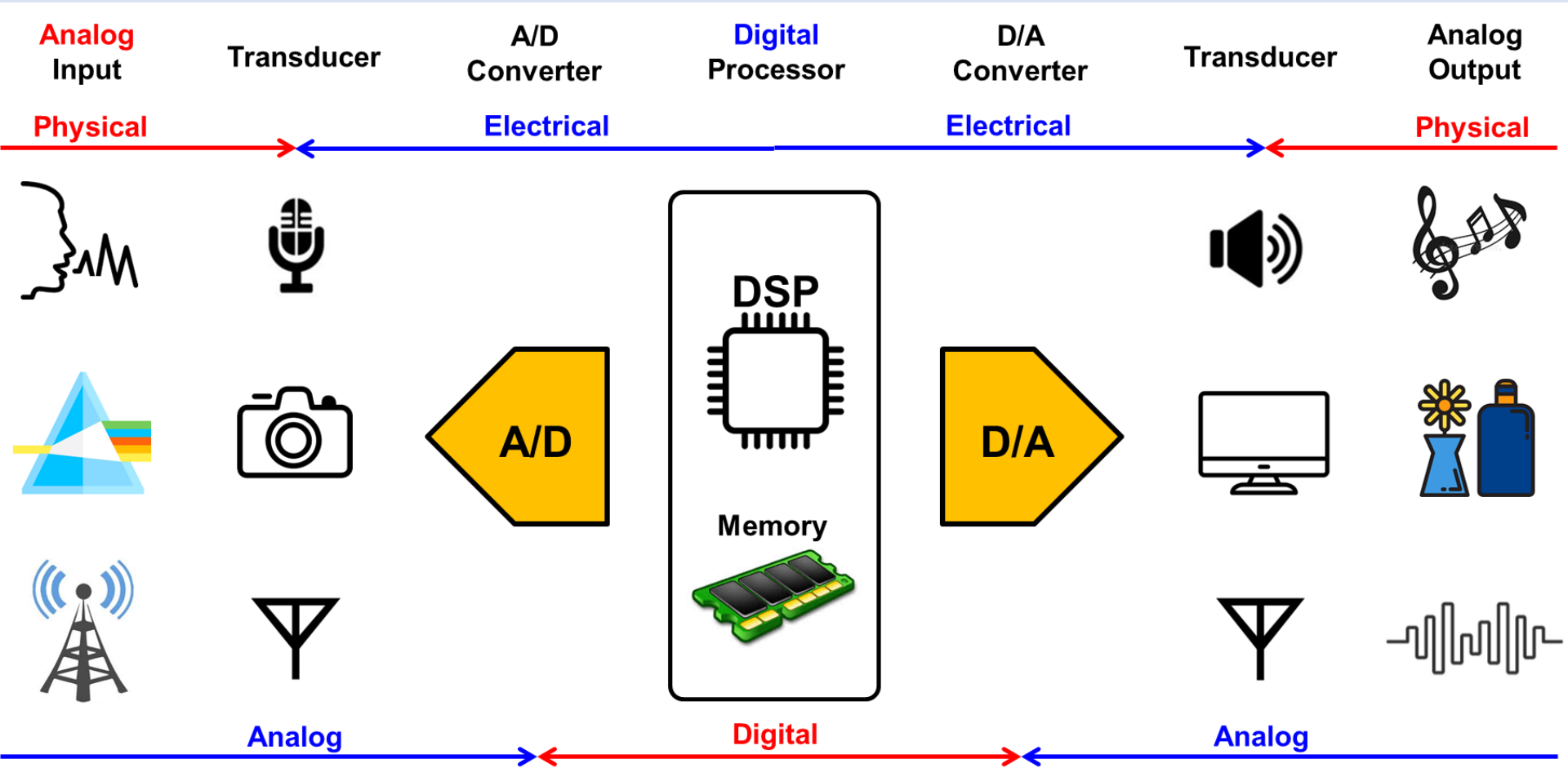

신우석





데이터 컨버터(ADC/DAC) 소개

ADC/DAC 필요성


Analog Input
Transducer
A/D Converter
Digital Processor
D/A Converter
Transducer
Analog Output
Physical
Electrical
Electrical
Physical
DSP
A/D
D/A
Memory
Analog
Digital
Analog

ADC/DAC 필요성

- 3 cameras
- LiDAR scanner

(LiDAR:
light detection and ranging)

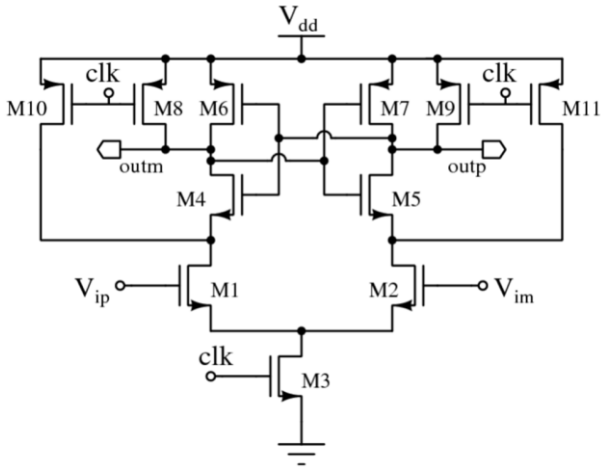
- infrared camera
- proximity sensor
- ambient light sensor
- front camera
- speaker
- microphone
- touch screen
- speaker
- microphone

- compass
- 3-axis accelerometer
- 3-axis gyroscope
- GPS

데이터 컨버터(ADC/DAC) 기본 구성

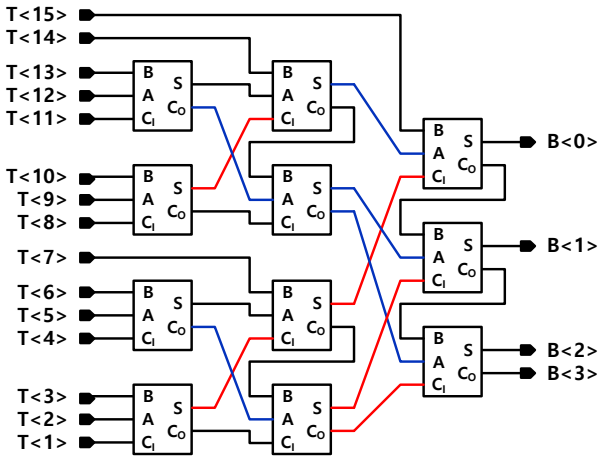
➢Analog Circuits

- Comparator
- Amplifier
- Sampler (T/H & S/H)
- Bootstrapped switch
- Voltage & Current bias



➢Digital Circuits

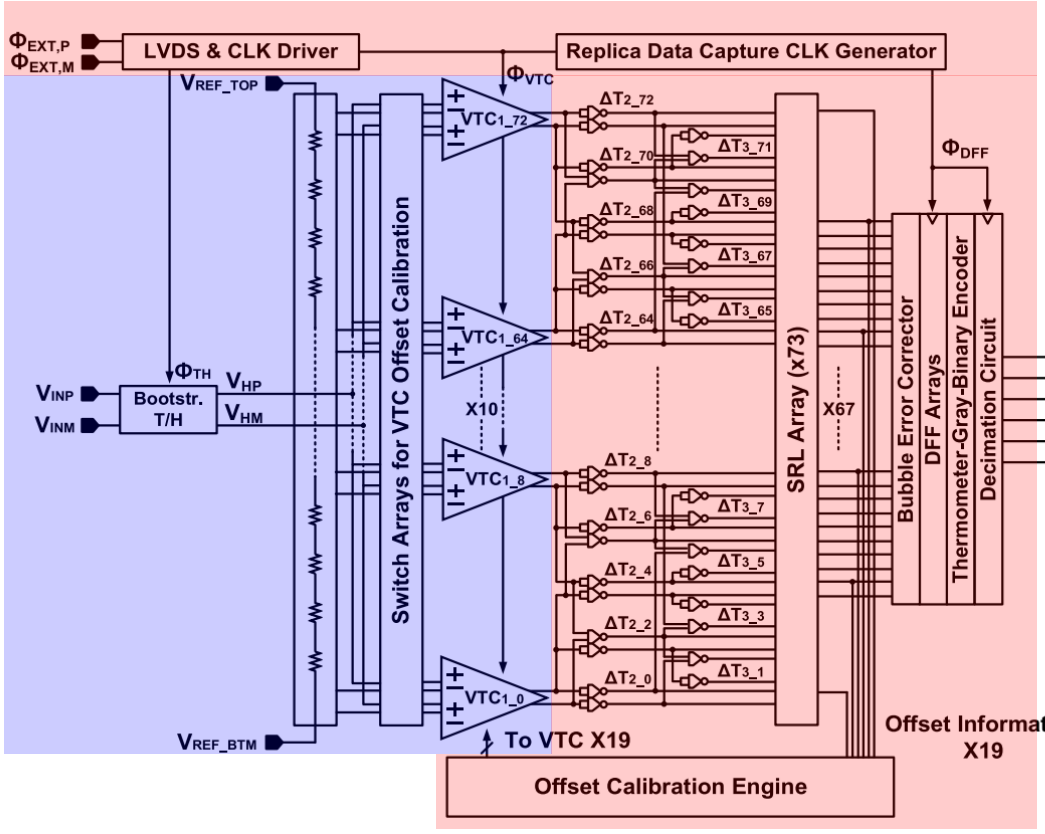
- En/Decoder
- Clock generator
- Digital calibration engine
- Decimator
- Output multiplexer



데이터 컨버터(ADC/DAC) 기본 구성

➢Flash ADC (D.-R. Oh, JSSC19')

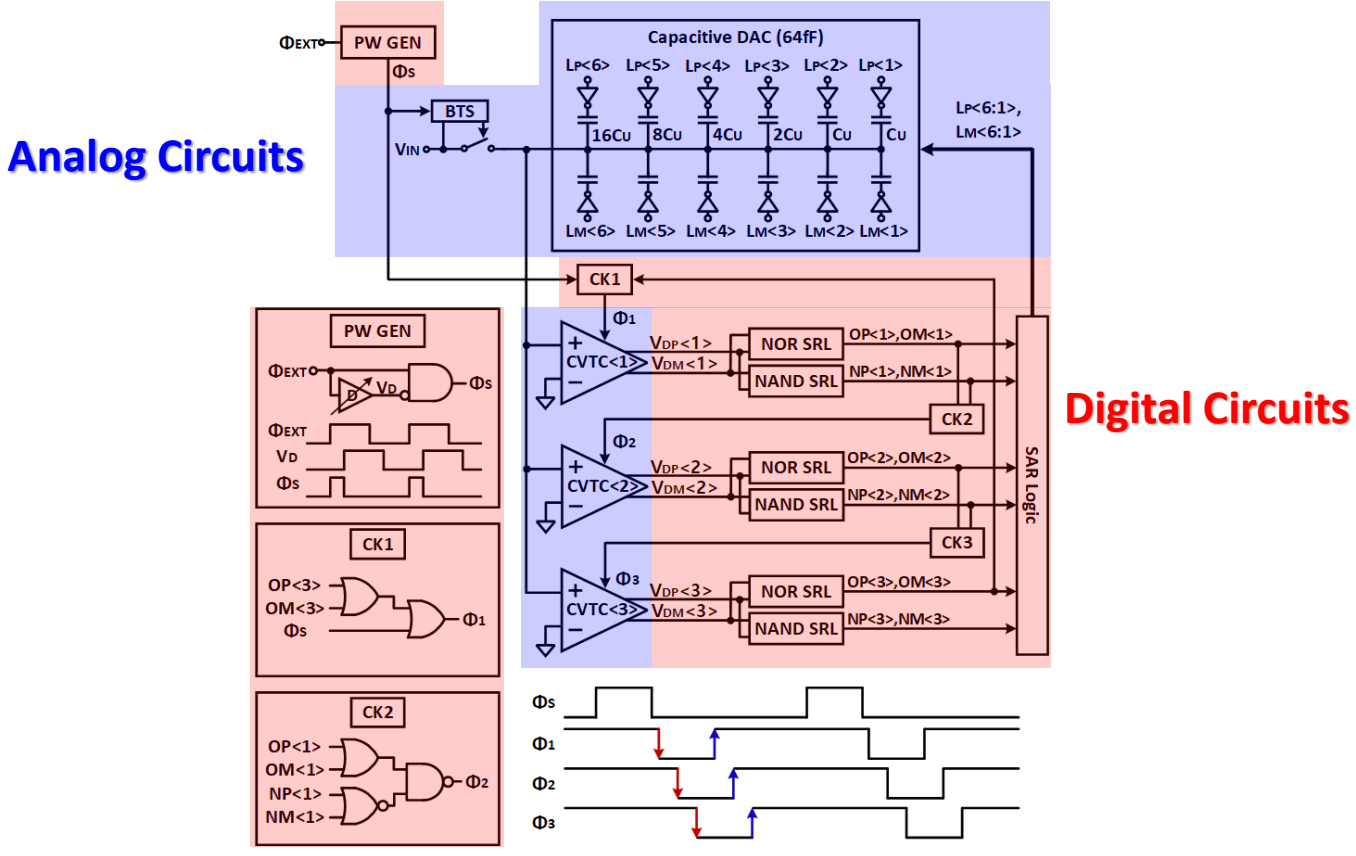
Analog Circuits



Digital Circuits

데이터 컨버터(ADC/DAC) 기본 구성

➢SAR ADC (D.-R. Oh, EL25')



데이터 컨버터(ADC/DAC) 설계 과정

Feasibility 검증
[MATLAB & Python]

↓

Schematic 설계
[Virtuoso&Spectre]

Layout 설계
[Virtuoso&PnR&Calibre]

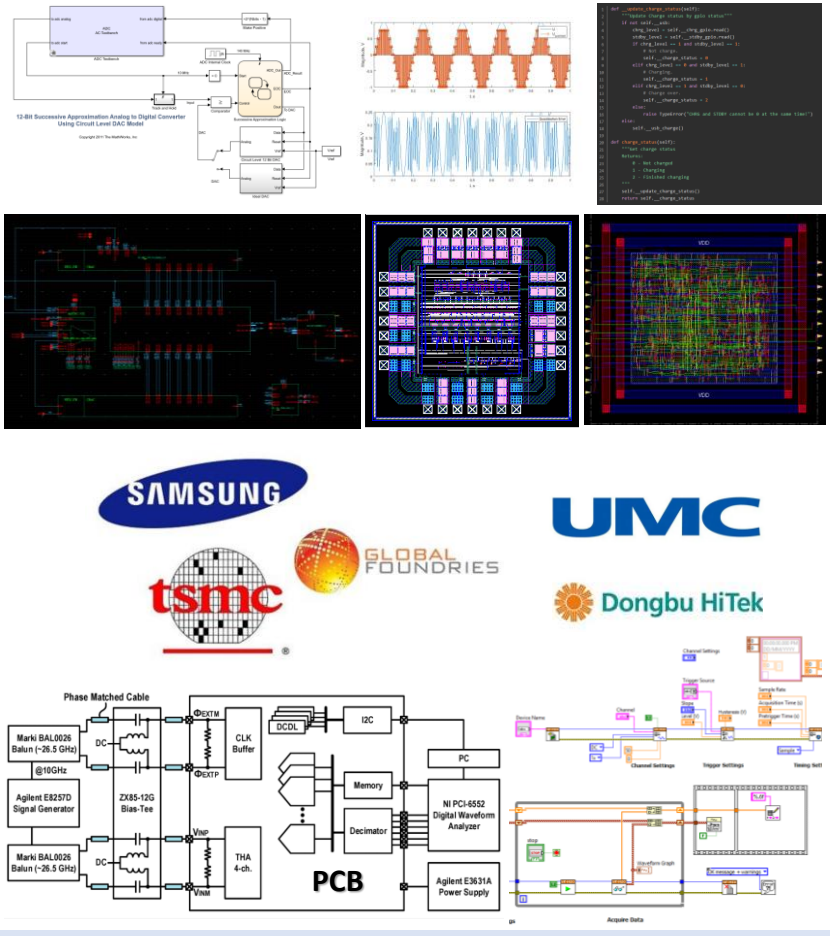
↓

MPW 칩 제작
[Foundry service]

↓

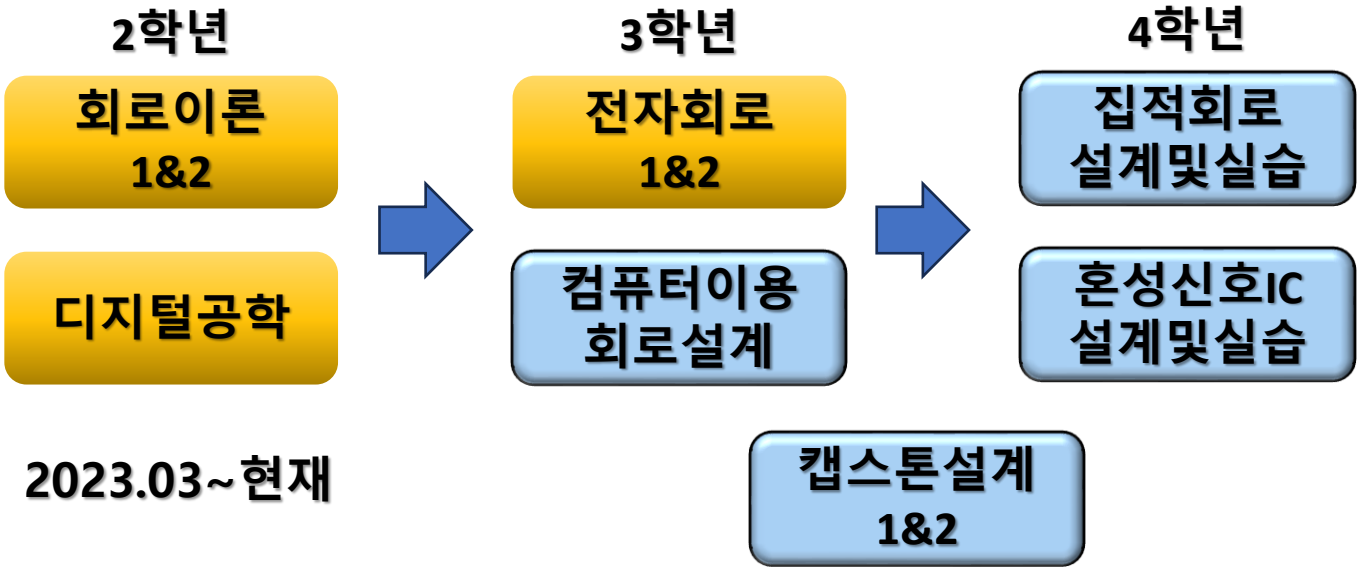
측정용 PCB 제작
[OrCAD]

성능 평가
[NI LabView]



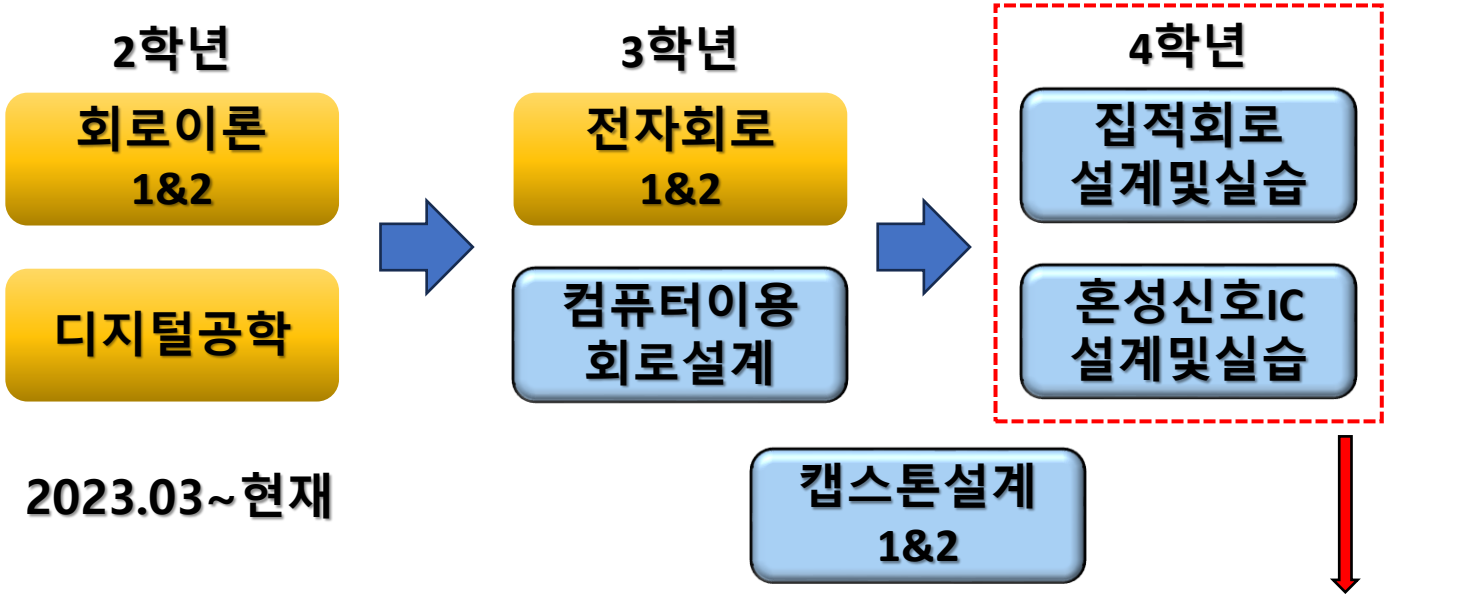
My Chip 서비스 활용 교육과정

제주대학교 전자공학과 반도체 회로교육과정



- ✓ **컴퓨터이용회로설계**: Analog circuits design (OrCAD+Bread board)
- ✓ **집적회로설계및실습:** Analog&Digital circuits design (Virtuoso, Spectre)
- ✓ **혼성신호IC설계및실습:** ADC design (Virtuoso, Spectre, Digital back-end)

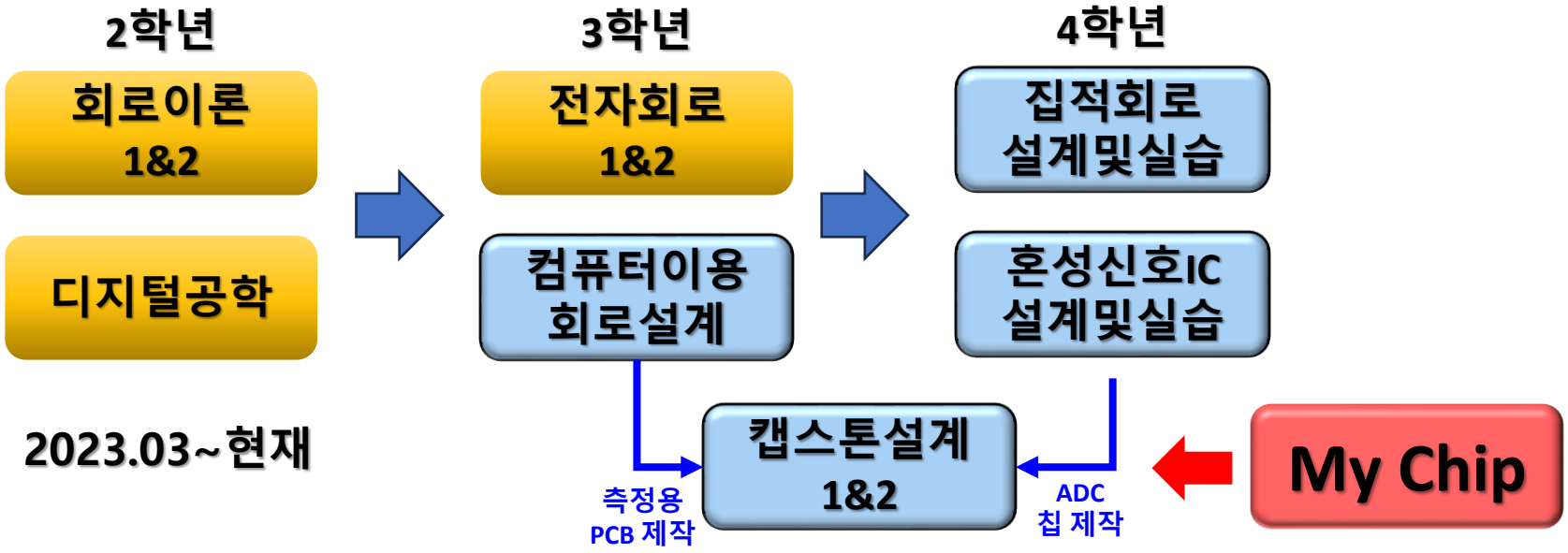
제주대학교 전자공학과 반도체 회로교육과정



IDEC SoC 설계과목 이수제 지정 교과목
(EDA tool 라이선스 지원)

- ✓ **Analog design:** Cadence Virtuoso&Spectre (Schematic&Layout)
- ✓ **Digital design:** Synopsys Digital Front&Back-end (Verilog&Auto PnR)
- ✓ **Layout design:** Siemens Calibre (RC extraction)

제주대학교 전자공학과 반도체 회로교육과정



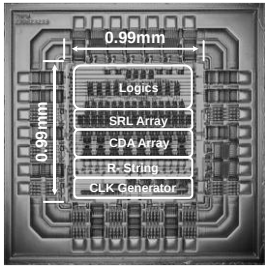
My Chip MPW Service 참여

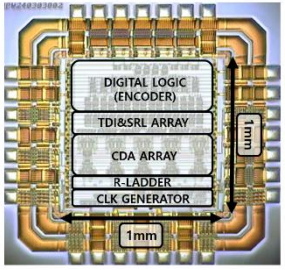
- ✓ Schematic 설계 ➔ Layout 설계 ➔ Chip 제작 ➔ 측정용 PCB 제작
- ✓ 1.5년 교육 과정 (교육과정 30명, My Chip 12명 참여)
- ✓ 23'~24': ADC 4종 MPW 칩 제작 및 측정 완료

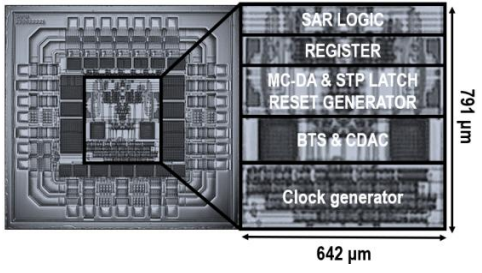
My Chip 서비스 기반 ADC IP 4종

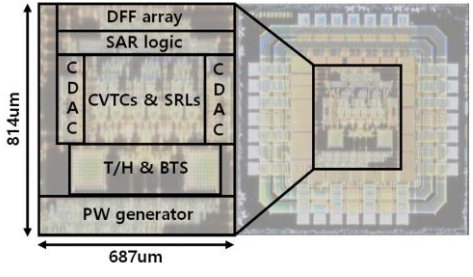
1. ADC 설계

- **ADC–1: 4-b 40-MS/s 2x IP Flash ADC**
  - 2023.11 MPW
- **ADC–2: 4-b 20-MS/s 4x IP Flash ADC**
  - 2024.03 MPW
- **ADC–3: 6-b 10-MS/s Sync. SAR ADC**
  - 2023.11 MPW
- **ADC–4: 6-b 10-MS/s Async. SAR ADC**
  - 2024.03 MPW





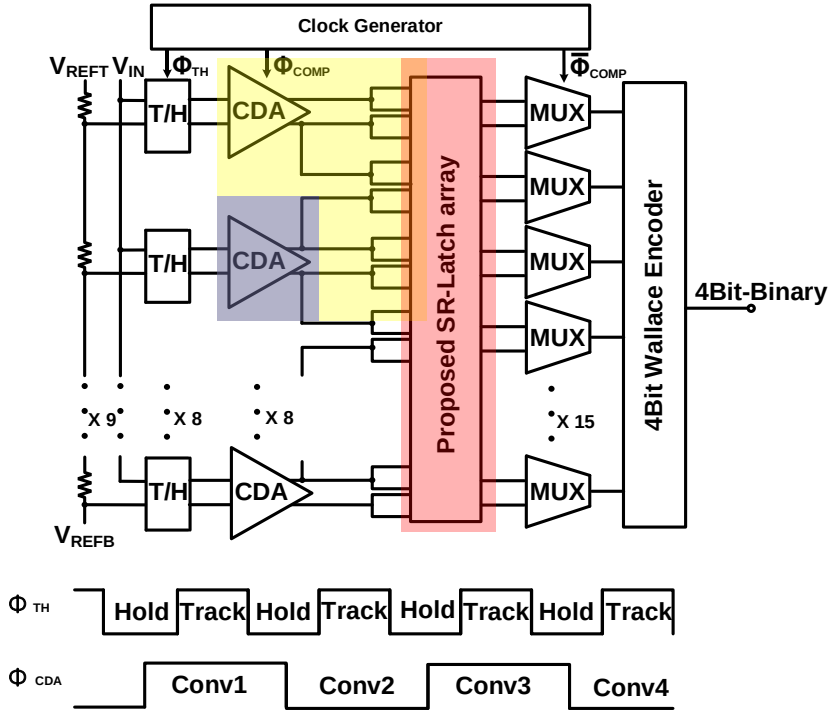




ADC-1: 4-b 40-MS/s 2x IP Flash ADC

➢Main idea

- Power-efficient dynamic amplifier
- 2-time time-domain interpolation
- Spurious latching prevention technique



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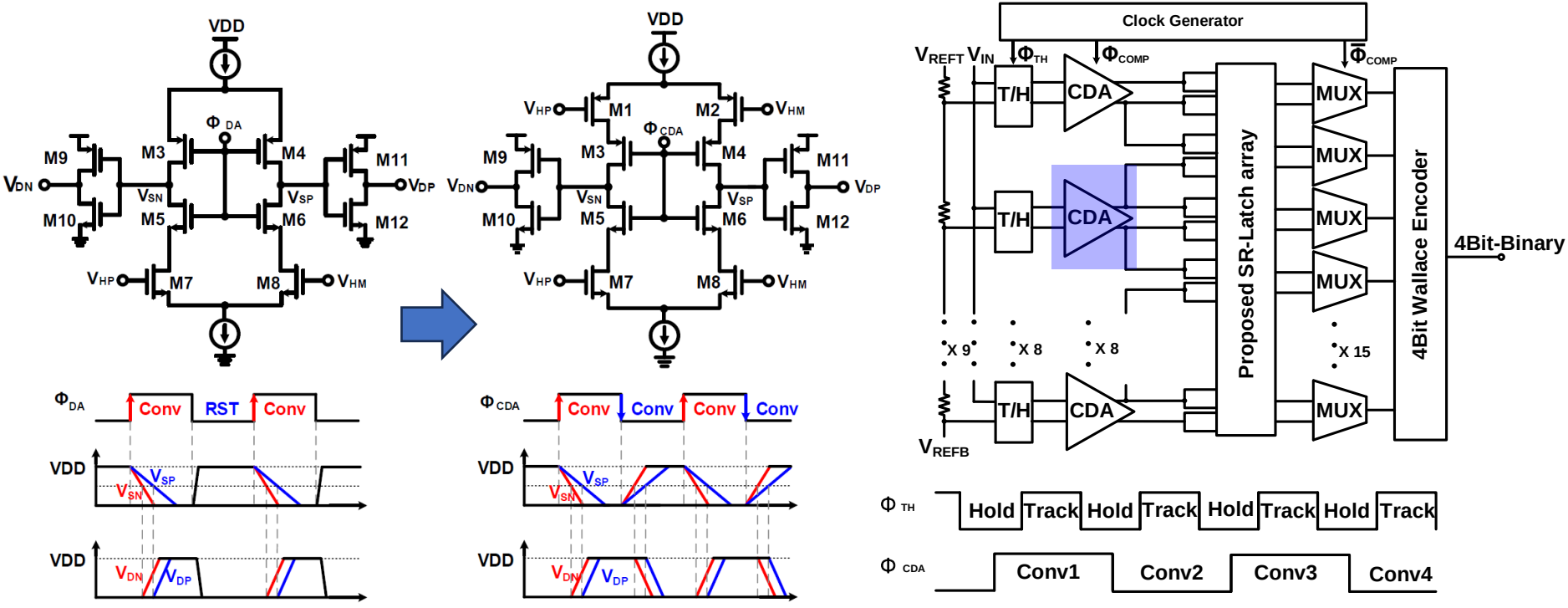
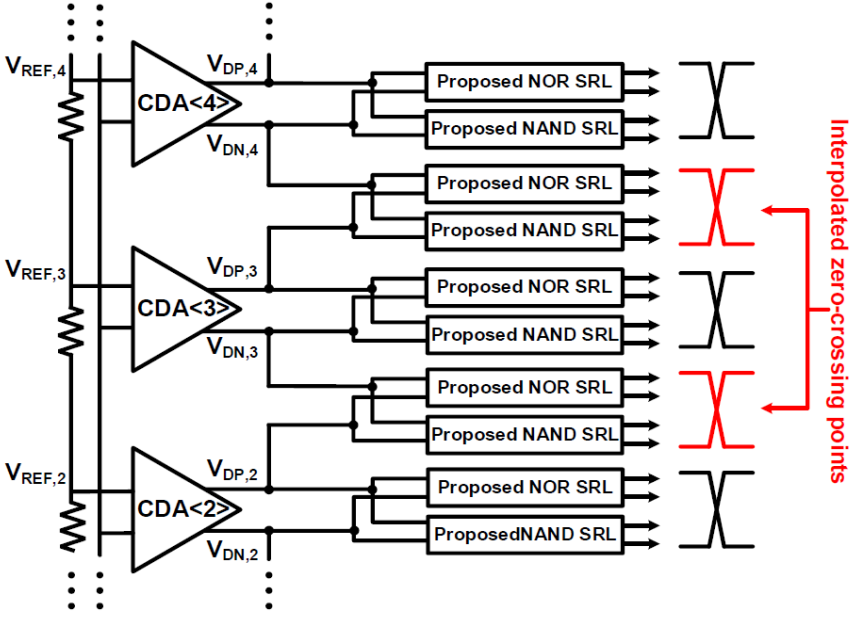
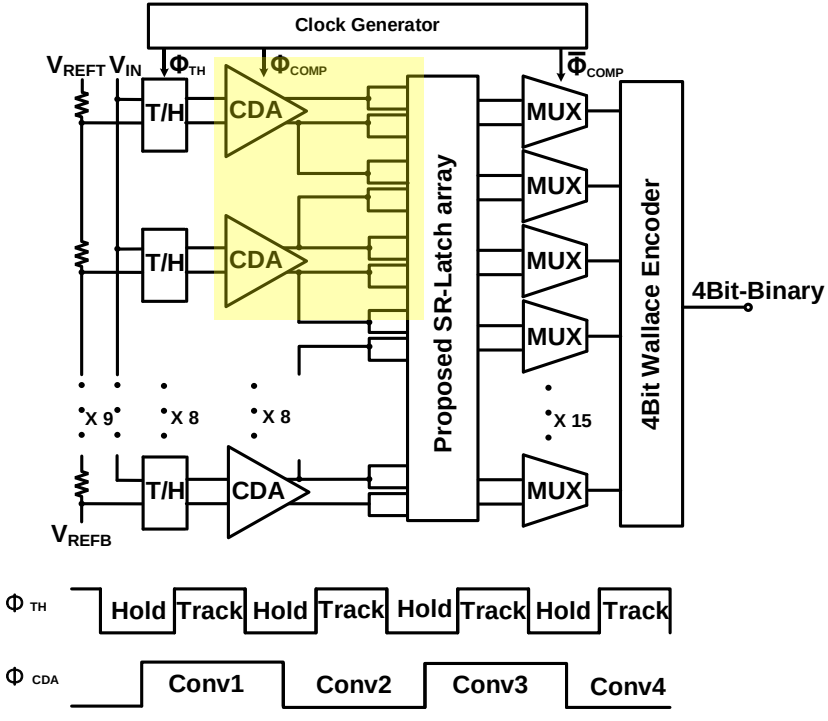


ADC-1: 4-b 40-MS/s 2x IP Flash ADC

➢Main idea

- 2-time time-domain interpolation





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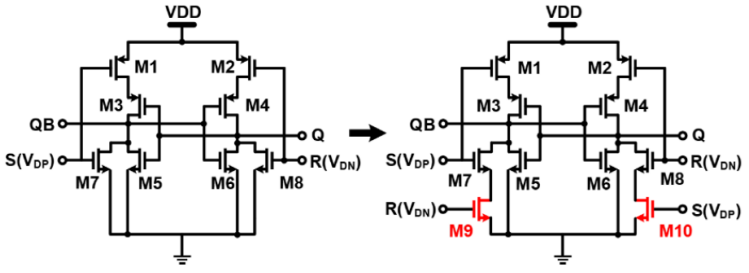
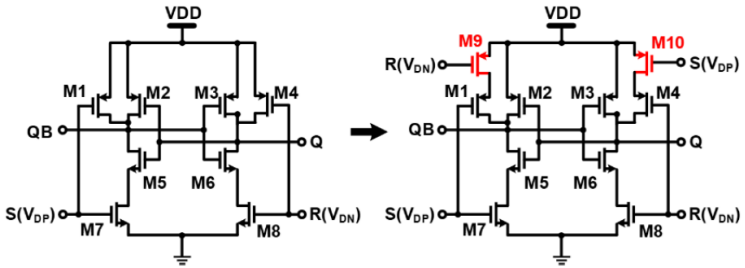
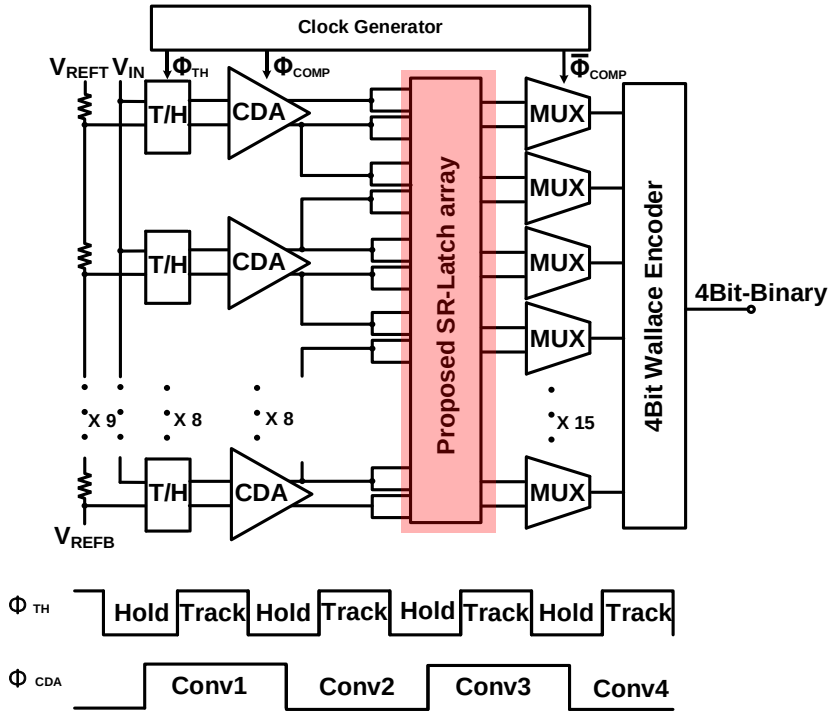
- Spurious latching prevention technique



[NOR-based SR-Latch]



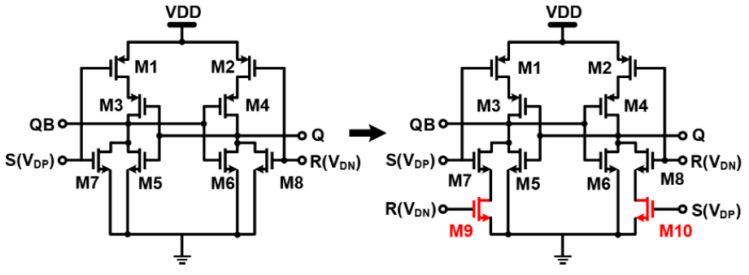
[NAND-based SR-Latch]



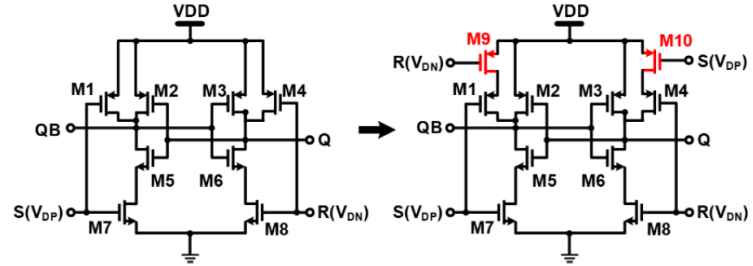
ADC-1: 4-b 40-MS/s 2x IP Flash ADC

➢Main idea

- Spurious latching prevention technique

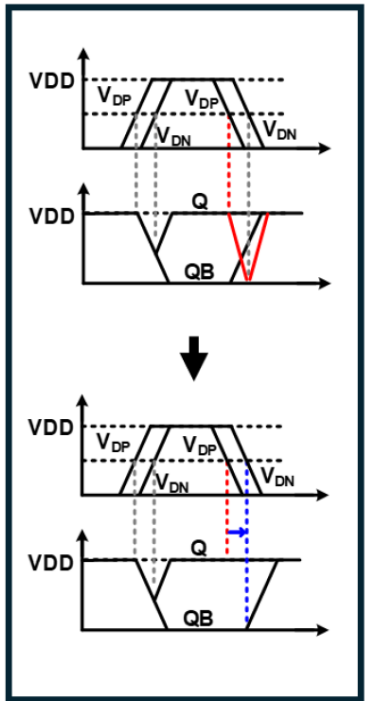


[NOR-based SR-Latch]

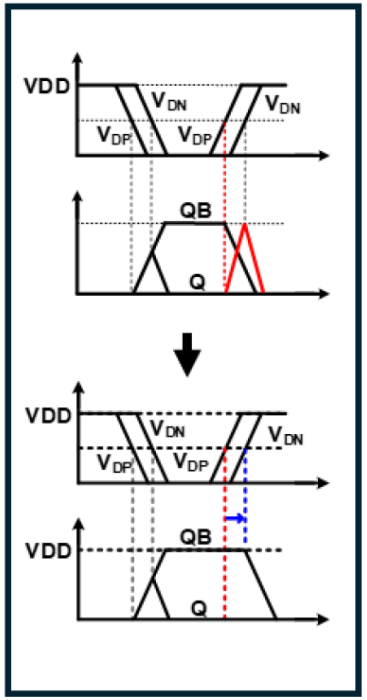


[NAND-based SR-Latch]

[NOR-based SR-Latch]



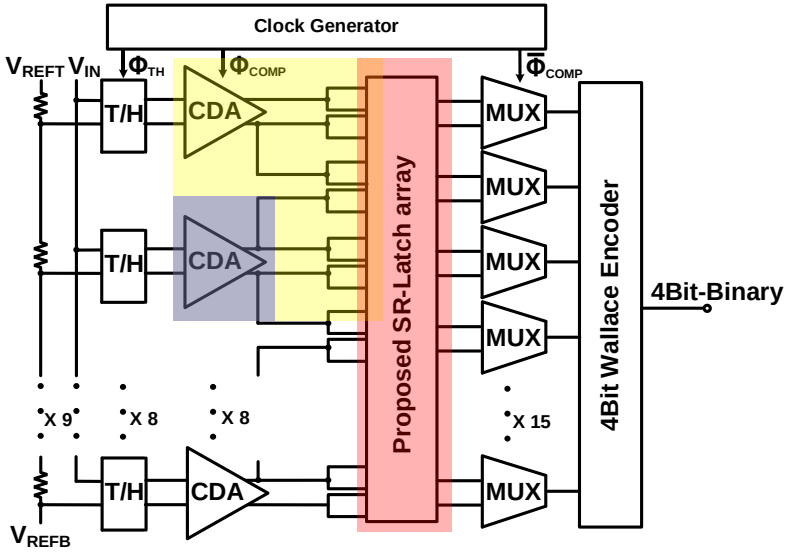
[NAND-based SR-Latch]

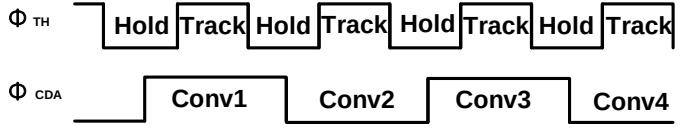


ADC-1: 4-b 40-MS/s 2x IP Flash ADC

➢ Advantages

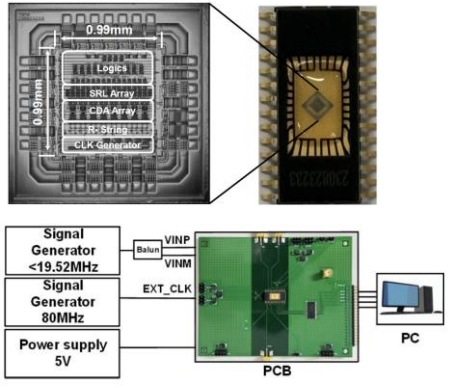
- Power-efficient dynamic amplifier
  - Low power
  - Reduce speed burden
    - ✓ SR-Latches
    - ✓ Comparator clock
- 2-time time-domain interpolation
  - 1st stage blocks: 15 ➔ 8
  - Compact area
  - Low power
  - Low input capacitance
- Spurious latching prevention technique
  - Stable latching operation





ADC-1: 4-b 40-MS/s 2x IP Flash ADC

➢Measurement results



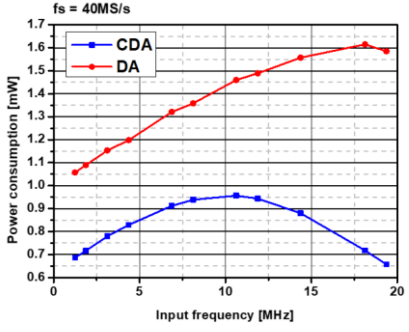
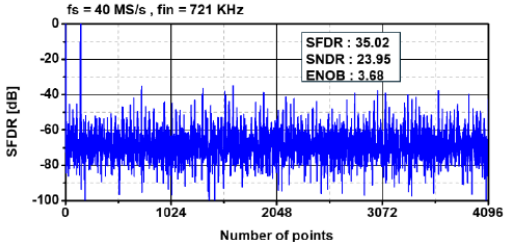
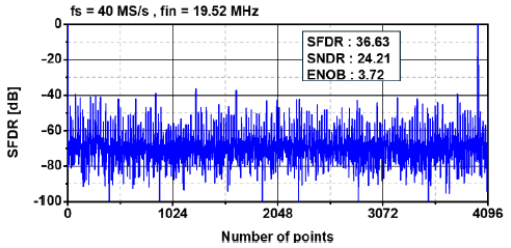
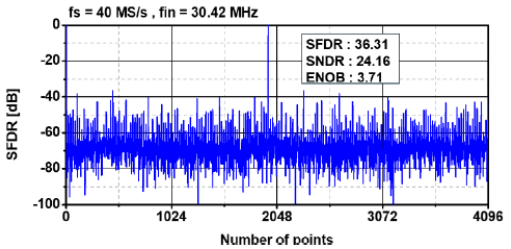


TABLE I
POWER BREAKDOWN

	DA-based Flash	DA-based IP Flash	CDA-based IP Flash
DA or CDA array	22.13 mW	11.16 mW (49.6%)	7.26 mW (67.2%)
CLK driver	9.2 mW	7.92 mW (13.9%)	5.73 mW (37.7%)
Track-and Hold(T/H)	4.35 mW	2.28 mW (47.6%)	2.28 mW (47.6%)
SRLs array	1.5 mW	1.59 mW (-0.1%)	656.4 uW (56.2%)
Encoder	5.02 mW	5.18 mW (-3.2%)	5.99 mW (-19.3%)
R-string	2.92 mW	2.92 mW	2.92 mW
Total	43.05 mW	31.05 mW (27.9%)	24.84 mW (42.3%)







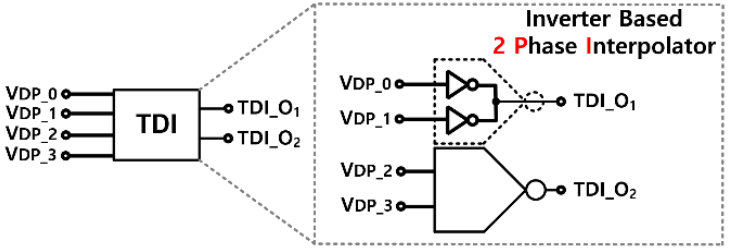
➢성과

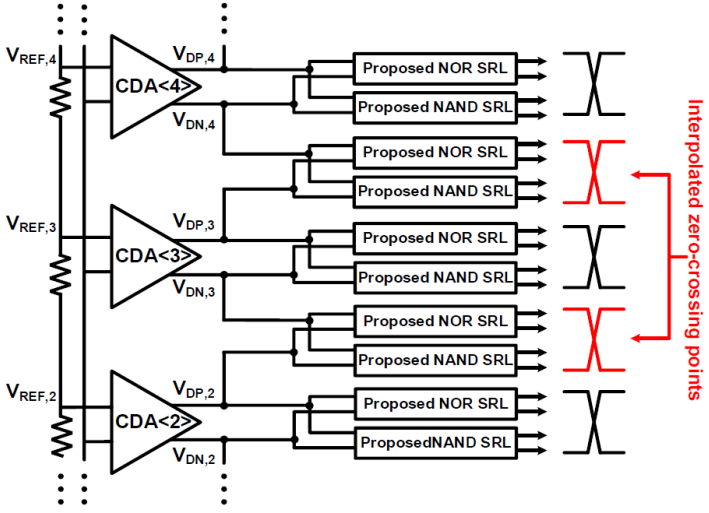
- 국내 학술대회 3편, 국내 특허 출원 1건
- 대학원 진학 1명 (My chip 3명 참여)

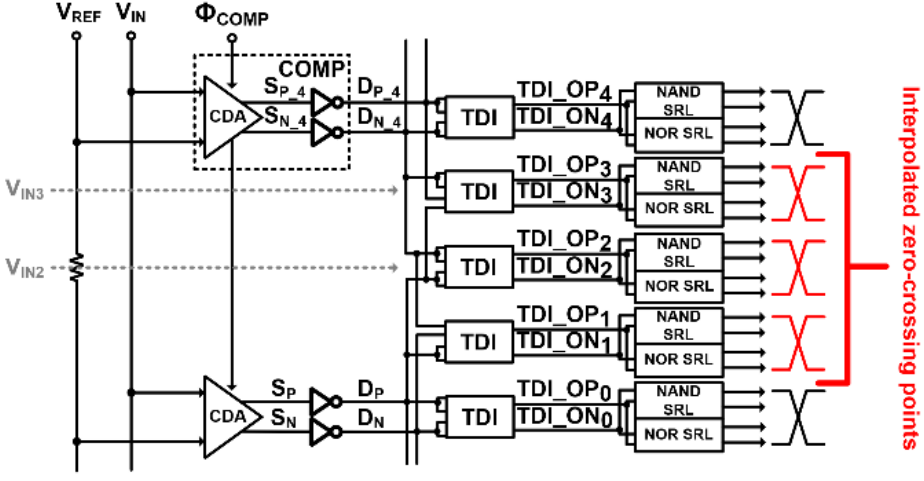
ADC-2: 4-b 20-MS/s 4x IP Flash ADC

➢Main idea (added compared to ADC-1)

- 2-times IP ➔ 4-times IP using inverter-based phase interpolator
- 1st stage blocks: 15 ➔ 8(2x) ➔ **5(4x)**
- Reduce input capacitance





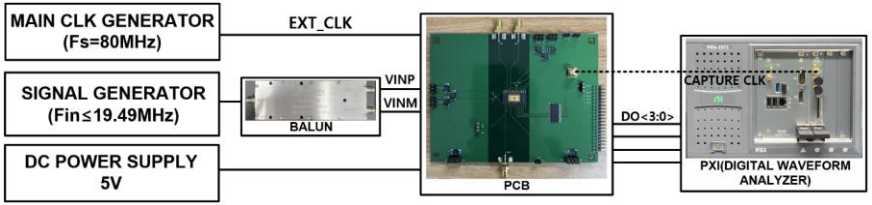


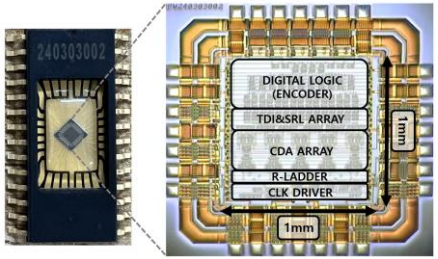
ADC-2: 4-b 20-MS/s 4x IP Flash ADC

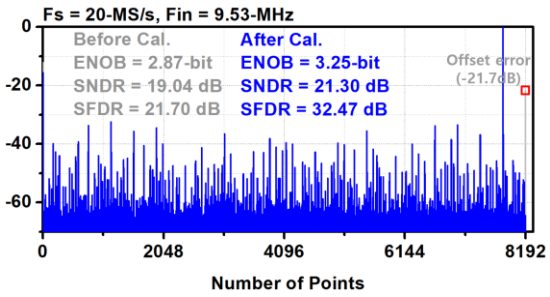
➢Measurement results

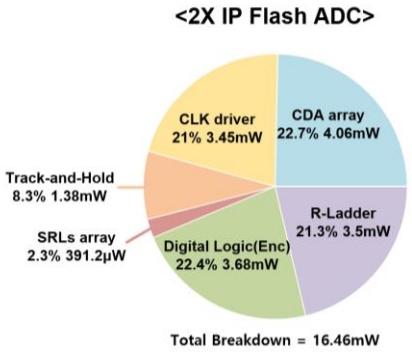
Architecture	CDA based 4 IP Flash ADC
Process	500nm CMOS
Resolution	4-bit
Sampling frequency	20-MS/s
Input Range	1.75 Vp-p Differential
Power Supply	5 V

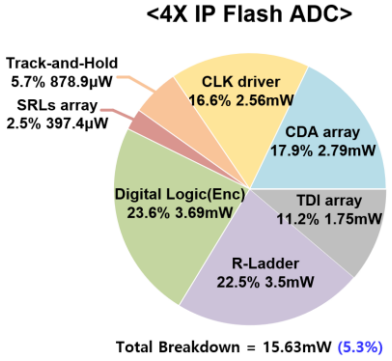
	Input capacitance (5-CDAs)	
2 Interpolated Flash ADC	Sampling Cap.	0.96pF
	Parasitic Cap.	1.92pF
	Total	**2.88pF**
4 Interpolated Flash ADC	Sampling Cap.	0.6pF
	Parasitic Cap.	1.23pF
	Total	**1.83pF (36.5%)**











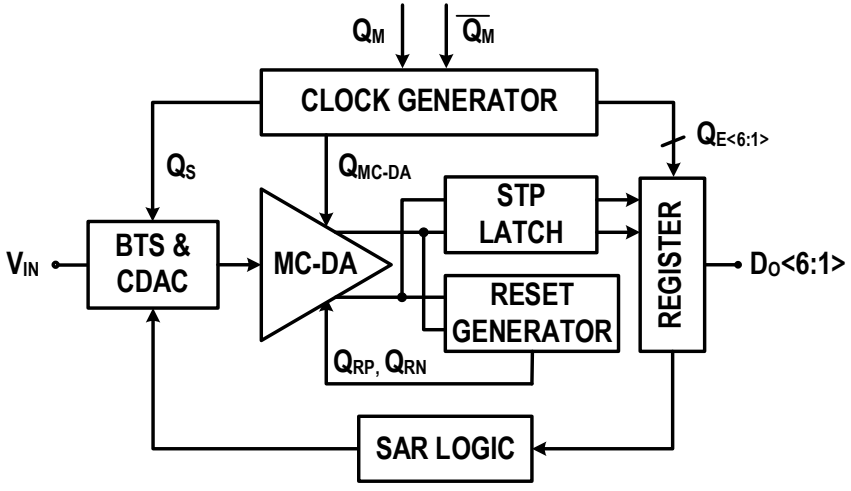
➢성과

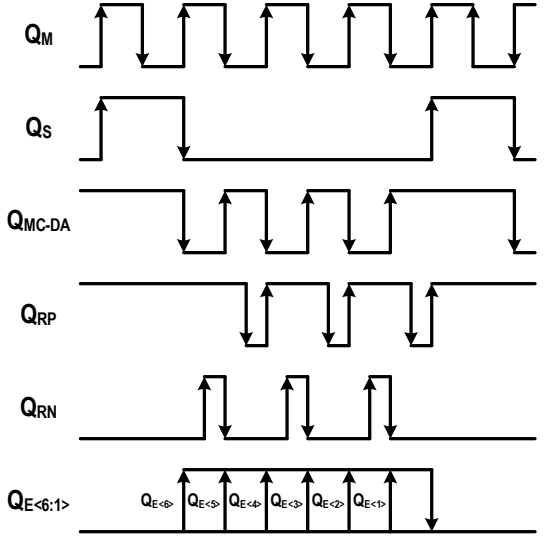
- 국내 학술대회 2편
- 대학원 진학 1명 (My chip 3명 참여)

ADC-3: 6-b 10-MS/s Sync. SAR ADC

➢Main idea

- Power-efficient dynamic amplifier with adaptive reset phase
- Reduce speed of comparator clock by half



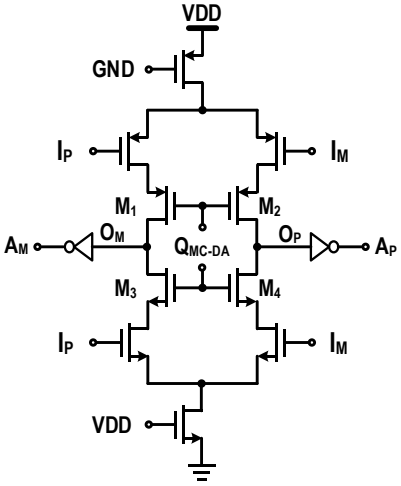


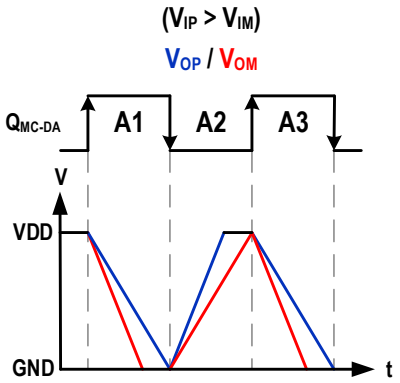
ADC-3: 6-b 10-MS/s Sync. SAR ADC

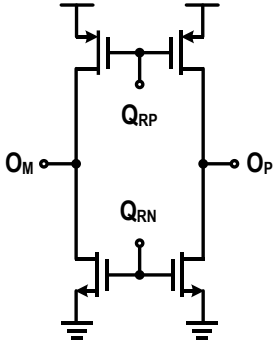
➢Main idea

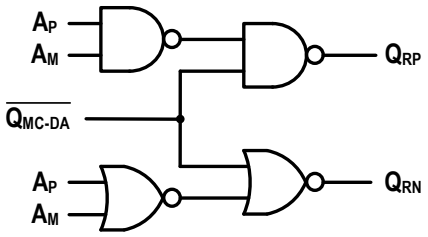
- Power-efficient dynamic amplifier with adaptive reset phase

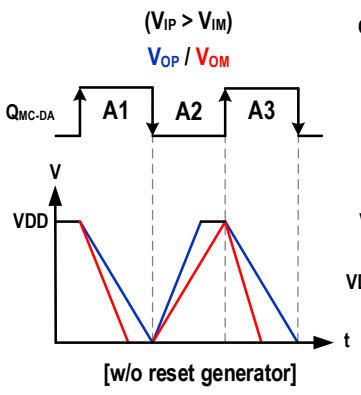
➔ Conversion speed enhancement

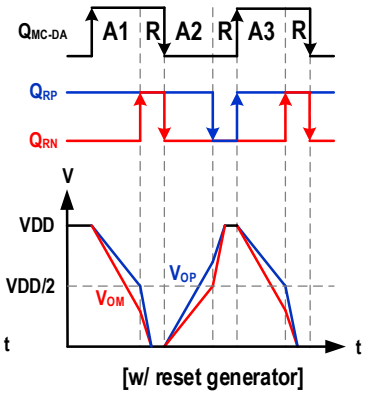






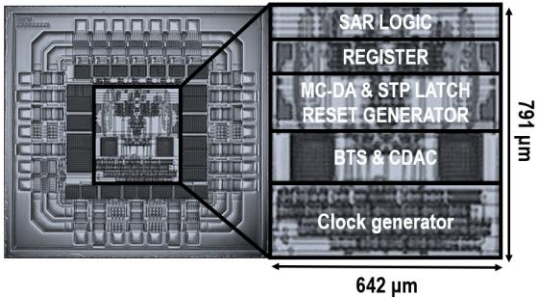




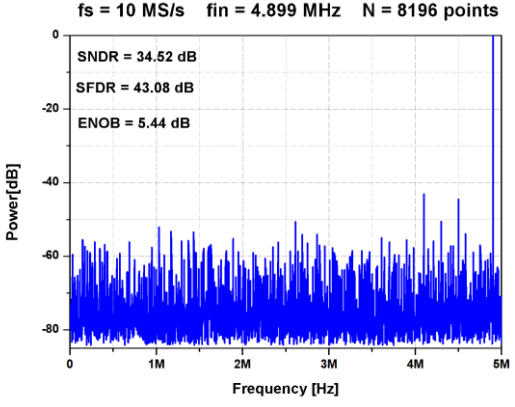


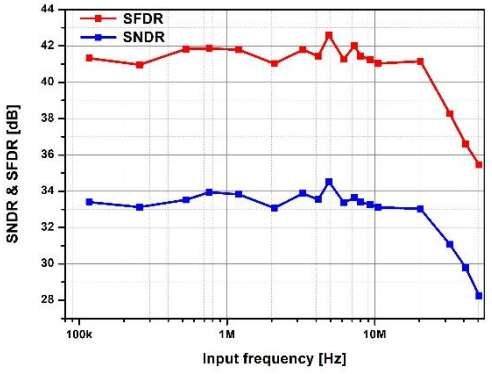
ADC-3: 6-b 10-MS/s Sync. SAR ADC

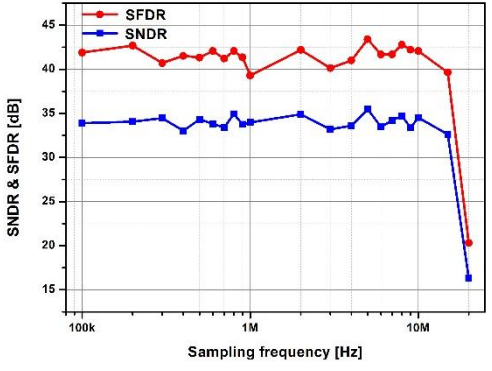
➢Measurement results



	DA based	MC-DA based	Power saving
BTS & CDAC	4.05 mW		-
Register & SAR Logic	2.55 mW		-
Pre-amplifier	9.80 mW	6.20 mW	36.73 %
SR-Latches	0.55 mW	0.66 mW	-16.67 %
Clock generator	6.04 mW	3.77 mW	37.58 %
Total	22.99 mW	17.23 mW	25.05 %







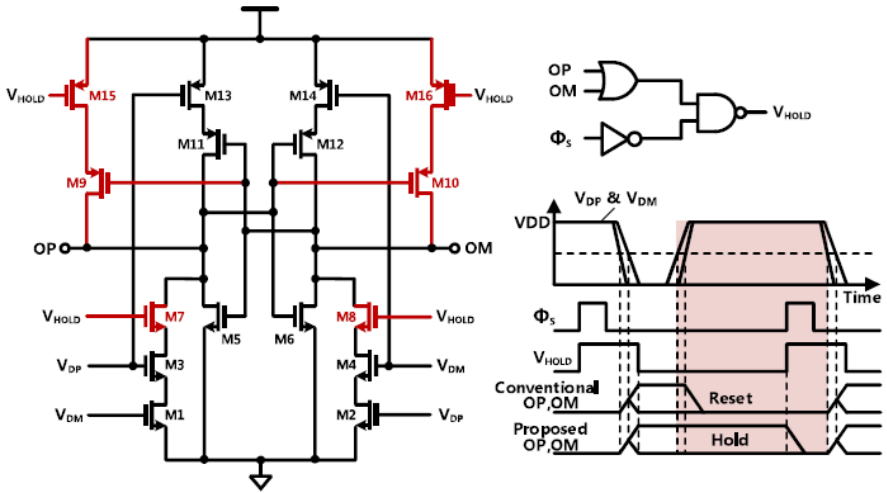
➢성과

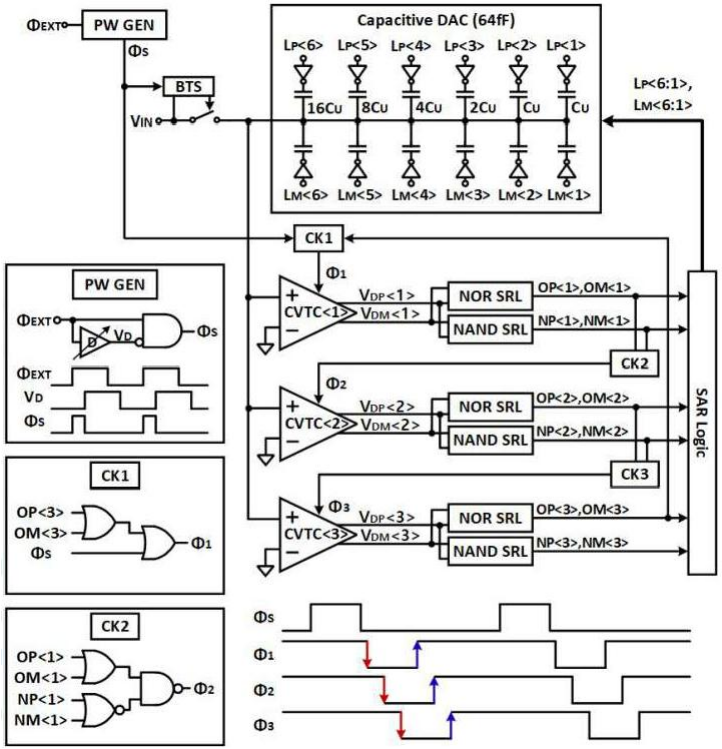
- 국내 학술대회 3편, 국내 출원 1건
- 대학원 진학 1명 (My chip 3명 참여)

ADC-4: 6-b 10-MS/s Async. SAR ADC

➢Main idea

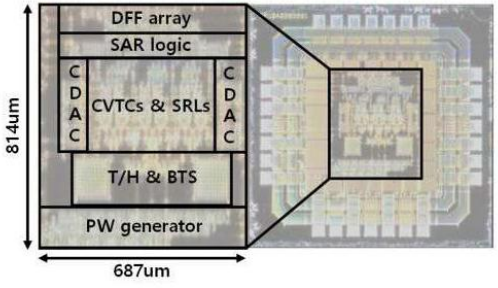
- Asynchronous loop-unrolled SAR ADC with power-efficient dynamic amplifiers
  - Only 3-DAs for 6bit resolution
  - Reduce design burden for Async. Clock gen.
- Retentive SR-Latch technique

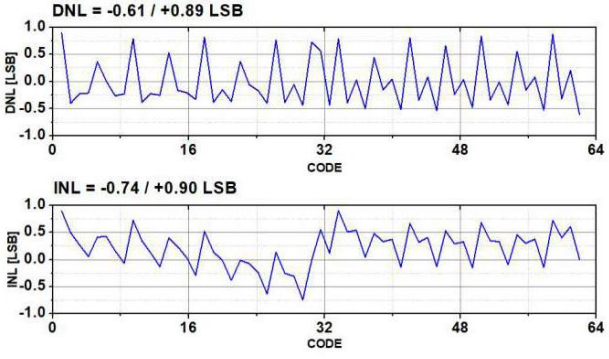


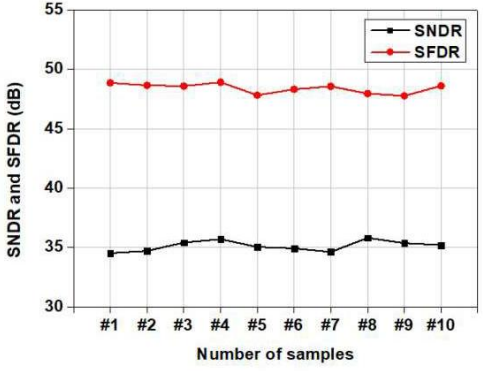


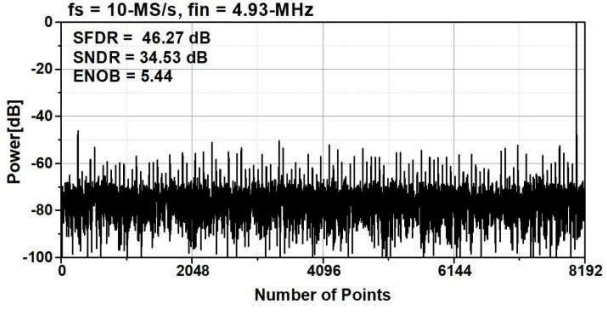
ADC-4: 6-b 10-MS/s Async. SAR ADC

➢Measurement results









ADC type	VTC-based	CVTC-based
Bootstrapped CDAC	0.91mW	
SAR Logic	1.08mW	
PW GEN	1.62mW	
CK 1~3	1.97mW	1.04mW
VTCs	4.51mW	2.75mW
SRLs	0.52mW	0.70mW
Total	10.61mW	8.1mW
Power saving	-	**23.66%**

➢성과

- 국내 학술대회 2편, 국제 학술대회 1편, 국내 출원 1건
- 대학원 진학 3명 (My chip 3명 참여)

결론 및 향 후 계획

결론 및 향 후 계획

- **실무 중심 학부 교육**
  - 회로이론 → 전자회로 → EDA tool 활용 설계 → 칩 제작 및 성능 평가
  - 학부생들이 혼성신호 집적회로에 대한 회로 설계 + 칩 제작 + 측정 경험 기회 제공
- **학부생 연구 논문 발표 및 특허 출원 기회 제공**
  - 국내 학술대회 10편
    - 2023년 대한전자공학회 전자정보통신 학술대회(CEIC2023) – 2편
    - 2024년 대한전자공학회 하계종합학술대회 – 4편
    - 2024년 대한전자공학회 RF&아날로그 워크샵 – 4편
  - 국제 학술대회 1편: IEIE ICEIC 2025
  - 국내 특허 출원 3건: 10-2023-0174253, 10-2025-0004518, 10-2023-0174265
- **대학원 진학률 상승**
  - My chip 서비스 12명 참여 ➔ 대학원(석사) 진학 6명
- **My chip 설계 계획**
  - 2025년 2차(6/10) MPW : ADC IP 3종 설계 진행 중
    - Multi-bit SAR ADC (1명), Flash-SAR ADC (2명), Pipeline ADC (3명)

감사합니다.