내 칩(My Chip) 제작 서비스 소개

National AI Research Institute –
Making a Better Tomorrow

2025.04.04.

초실감메타버스연구소
반도체소부장기술센터

노태문 연구전문위원

01. 반도체소부장기술센터 소개

반도체실험실 개요

반도체 일괄공정 연구시설을 통한 ICT 소재·부품·장비 산업 국가 경쟁력 강화 및 기술 선도

연혁

- **국내 최초 반도체 종합실험실 조성** (Since 1981, KIET)
  (청정실 776m² (5인치 실리콘) 1988년 → 청정실 1,430m², 현재)
- **실리콘실험실 6인치 증설** (청정실 930m², 2009년)
- **국내 최초 화합물 전용 실험실 조성** (3인치, 1991년)
- **화합물실험실 4인치 증설** (청정실 500m², 2000년)

현황

- **반도체실험실 : 2연구동 및 4연구동에 위치**
- **5,785m² 크기 실험실에 2,000여종의 연구장비 보유**

주요 성과

- **국내 반도체 산업의 산실 (4M/16M/64M DRAM 개발)**
- **차세대 소재부품 국가 연구개발 과제 지원**
  매년 100여개 이상 연구과제에 활용
- **산·학·연 국가 연구 및 기술 개발 인프라 제공**
- **중소기업의 기술 파트너**
  1993년부터 매년 50여개의 중소기업 기술 및 양산 지원
- **총 63조원의 경제적 파급효과**
  DRAM 분야 54조원 외 디스플레이, 통신 등의 누적 규모

반도체실험실 (Since 1981)

- **실리콘반도체 실험실(930m²)**
  - Si CMOS 일괄 공정 가능

- **디스플레이, 융복합센서 특화 실험실**
  - Nano Devices, OLED, 산화물반도체 소자 기술 개발

- **첨단 개별연구실험실(60개 LAB, 4,090m²)**
  - Organic Electronics, 나노 전자원, Tera Hertz Device, Bio, Optical Devices, Solar Cell, CAD, Measurements)

- **화합물실험실(500m²)**
  - 광소자 및 화합물 소자 개발

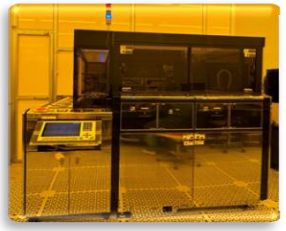
- **물성분석 및 패키징 실험실(265m²)**

01. 반도체소부장기술센터 소개

반도체실리콘 장비 요약

주요장비	제조사/모델명	주요 사양
I-Line Stepper		○ Resolution : 350nm, Alignment Accuracy : 70nm or better(LSA, FIA) ○ Exposure Area : 22mm square, Reduction Ratio : 1:5 ○ Numerical Aperture : 0.63, Reticle : 6 inch
Track System		○ Adhesion Treatment(HMDS) on Substrates ○ Photo Resist Coating ○ Development(TMAH) : Puddle & Spray ○ Hot Plate Baking
Dry Etcher		○ Oxide Etch, Nitride Etch, Poly-Si Etch, Metal Etch ○ PR Strip
Wet Station		○ Standard Cleaning, SC1 Cleaning, HF Cleaning, DI Cleaning ○ H_3PO_4 Etch : Nitride Strip ○ Wet Etch : Oxide Etch, Metal Etch ○ PR Strip : Acid PR Strip
LPCVD		○ TEOS Oxide, Nitride, Low Stress Nitride ○ Poly Si/Amorphous Poly Si, LTO, HTO, SION
PECVD		○Oxide, Nitride, TEOS, SACVD BPSG, Ge Oxide
Sputter		○ Al-1%Si, TiW , NiV, Cr, Mo ○ Ti, TiN, AlN, NbN
Furnace		○ Alloy, Wet/Dry Oxidation, Anneal, Drive-in ○ Dry Oxidation, Anneal, POCl3 Doping : 800 ~ 900℃
Ion Implant		○ Medium Current Ion Imp ○ High Current Ion Imp


I-Line Stepper


Track System


Dry Etcher


Wet Station


LPCVD/Furnace


Ion Implant


PECVD


Sputter

01. 반도체소부장기술센터 소개

실리콘 반도체실험실 히스토리

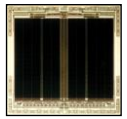
1981 실리콘실험실 개소
- 4동 G층 235평
- 실리콘 5인치

1982 전자기술연구소 국내 최초 32k ROM 개발

1988 국내 최초 4M DRAM 개발

1989 5인치 1.2㎛ CMOS 개발

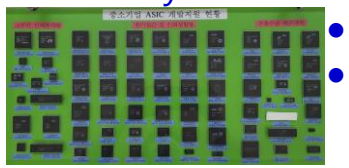
1990
- Dual Port SRAM



- 3.3V 10bit ADC
- 5.0V 10bit ADC

- IMA1.0

- Gate Array

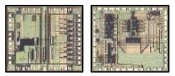


1993 CMOS 기반 원외 반도체기술지원

1995 5인치 0.8㎛ CMOS 개발

1996 Power 반도체 개발

1999 CDMA 및 ATM용 통신용 칩 개발
- IMA2.0
- IMA2.1
- 155 M Tx v4.0, Rx v4.0
- 155 M No Clock Rx
- 622 M bit Sync. Rx1
- 622 M Rx1, 622 M Rx2
- 622 M Tx1, 622 M Tx2

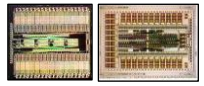


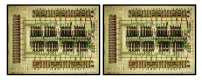
2001 5인치 0.5㎛ CMOS IC 개발

기술창업 ㈜알에프세미

실리콘 6인치 증설

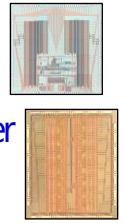
5인치 0.5㎛ AP IC CMOS 개발
- PDP Scan Driver
- PDP Data Driver
- FED Gate Driver
- FED Cathode Driver





2003 DC-DC Converter

- OLED Gate Driver
- OLED Source Driver



2008 6인치 SiC 전력반도체 기술 개발

실리콘 포토닉스 개발

지능형 실감 센서 개발

2013

2017 모노리틱 Si MIT Transistor 개발

2018 6인치 0.5㎛ AP (아날로그 파워) CMOS IC 개발

2021 6인치 0.5㎛ 아날로그 CMOS IC 공정/PDK 개발

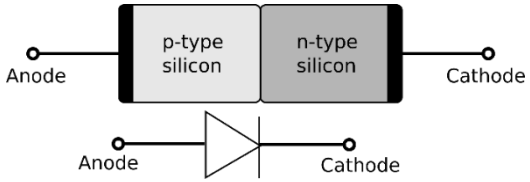
2022 6인치 0.5㎛ MPW 제작 지원

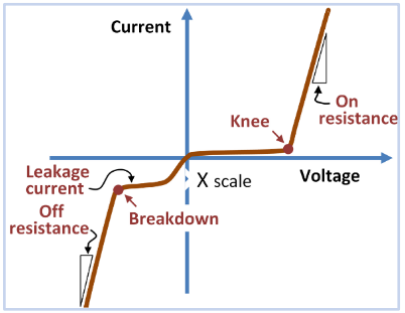
2023

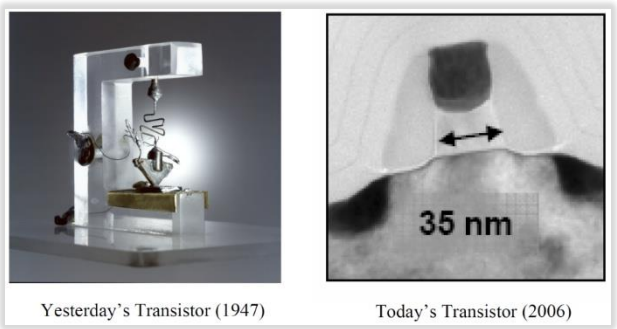
02. 반도체 소자 및 IC

반도체 소자

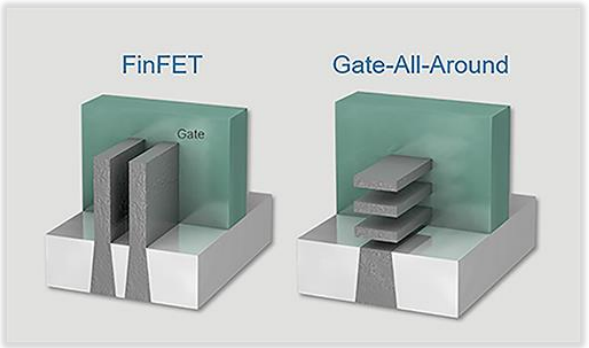
Diode





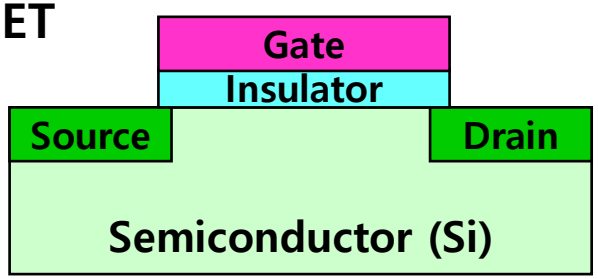


<John Bardeen, William Shockley and Walter Brattain>

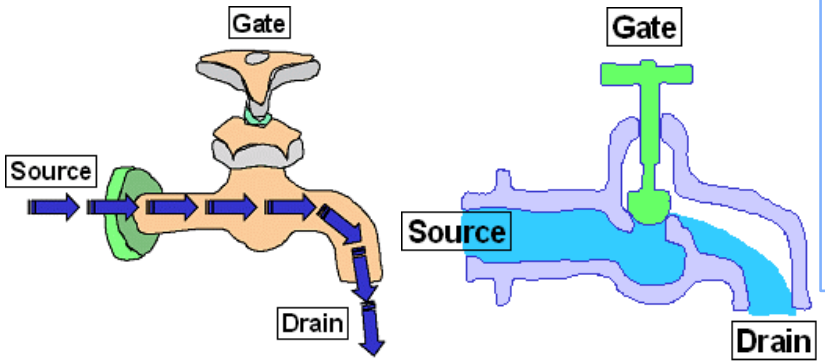


3D 반도체 구조인 핀펫(왼쪽)과 GAA(오른쪽) 비교.
[출처: 어플라이드머티어리얼즈]

MOSFET

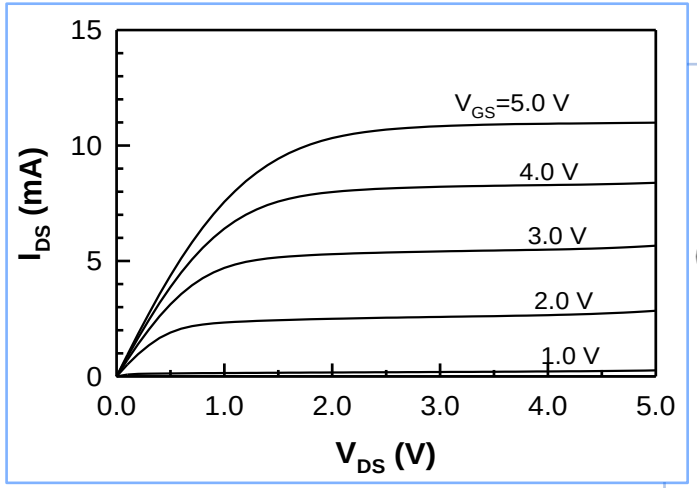


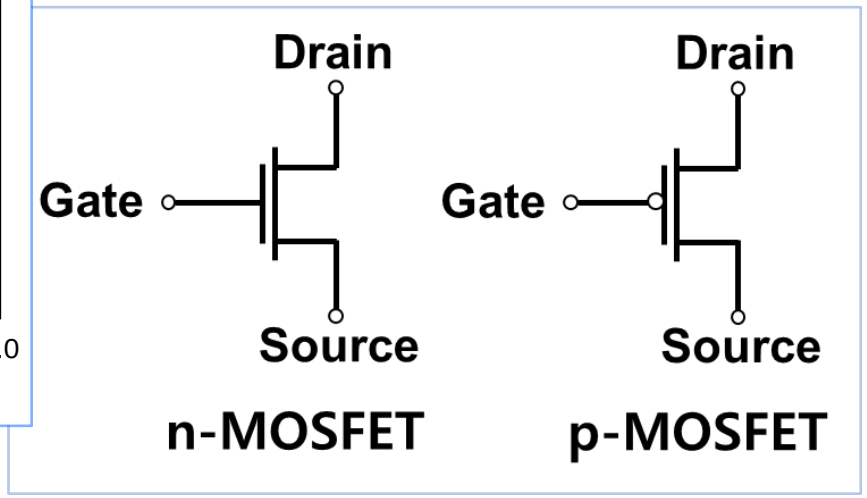
<MOSFET Structure>



<Concept of MOSFET>

※MOSFET: Metal-Oxide Semiconductor Field Effect Transistor

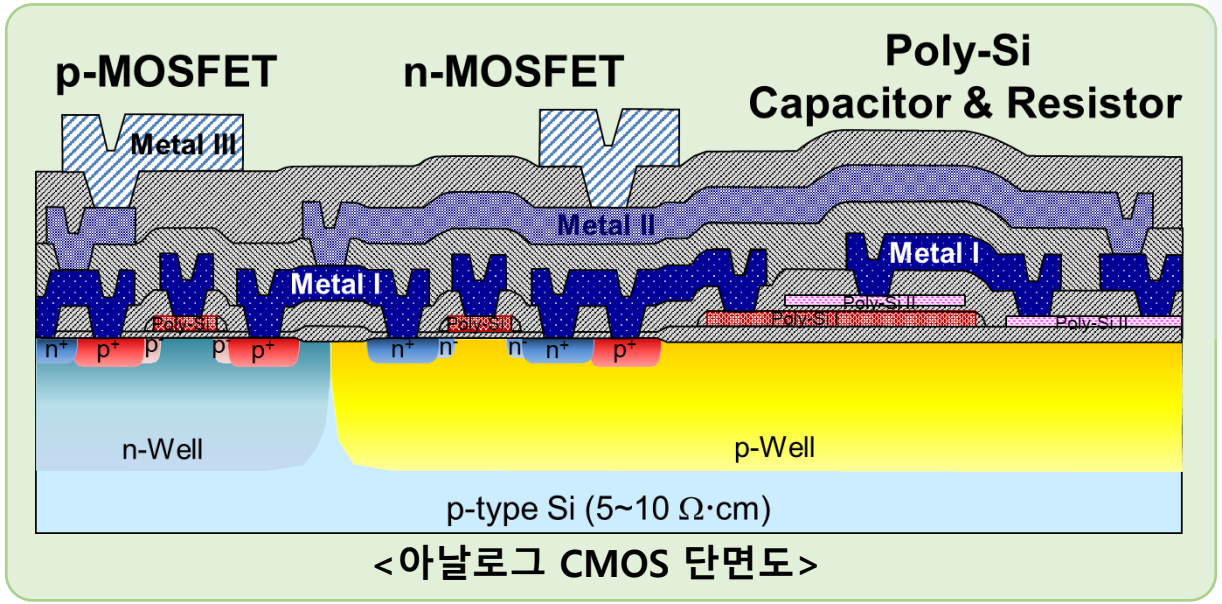




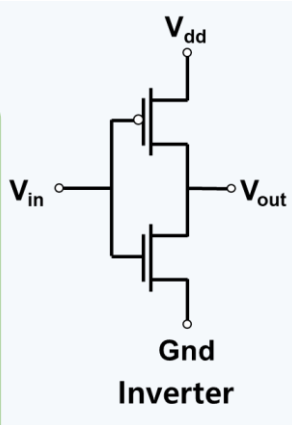
ETRI 한국전자통신연구원

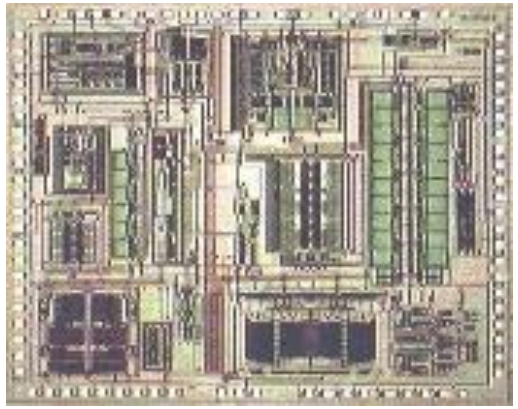
반도체 IC

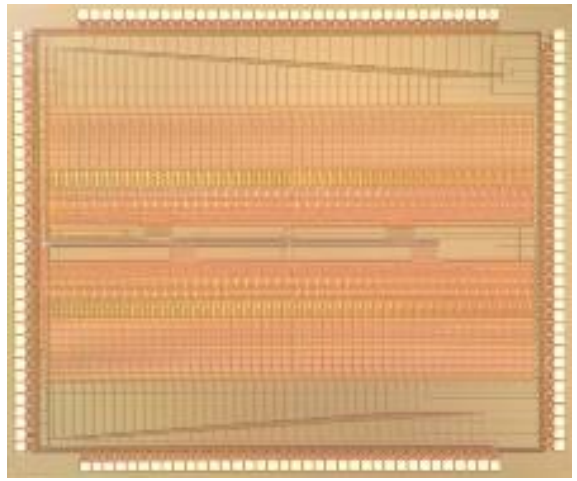
- IC



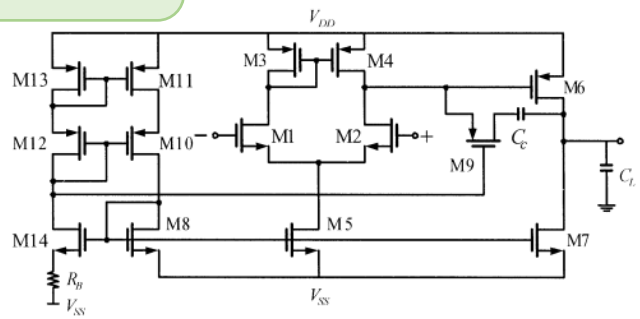
<아날로그 CMOS 단면도>







<ICs>



<Two stage CMOS Opamp (Operational Amplifier)>

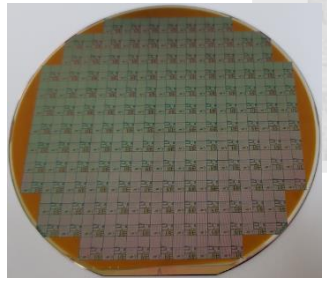
*IC: integrated circuit

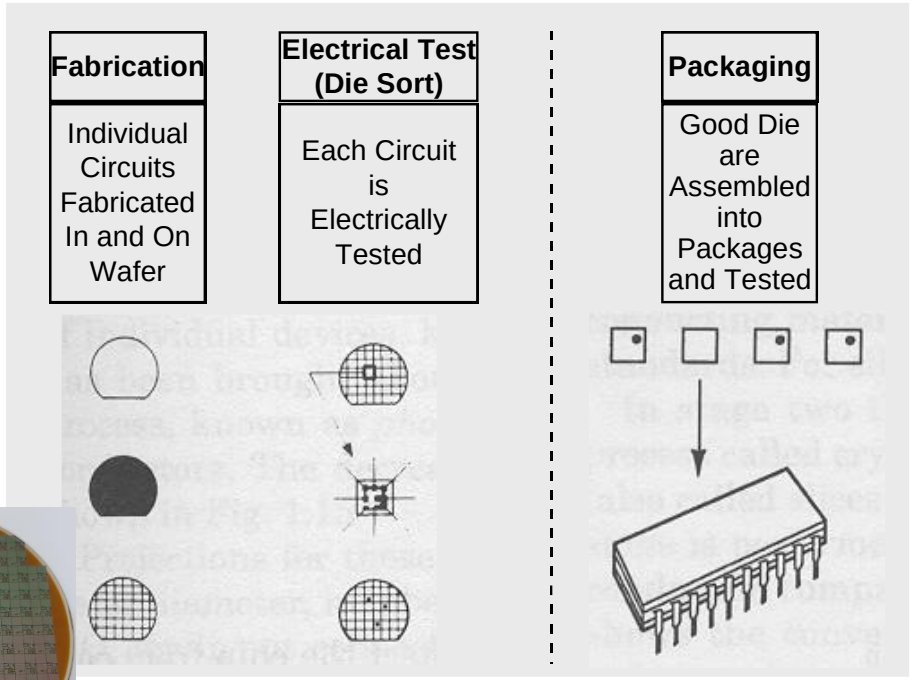
반도체 소자 제작 공정

- **Broad Sense**
  - Material preparation ➔ Crystal growth & wafer preparation ➔ Wafer fabrication ➔ Packaging

- **Fabrication Step**
  - Growing Si, GaAs, InP, GaN, etc.
  - Wafer preparation
  - Wafer fabrication
    - Deposition
    - Photolithography
    - Etching
    - Diffusion
    - Oxidation, etc.
  - Chip Test, Sorting and Packaging

- **Narrow Sense**
  - Wafer Fabrication

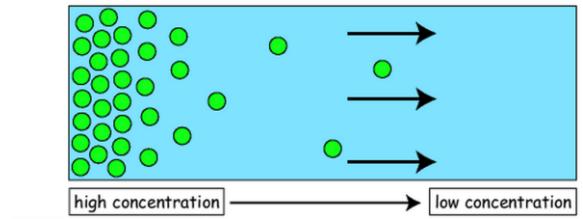




03. 반도체 공정

단위 공정 요약

- **Diffusion (확산)**
  - A physical phenomenon where particles such as impurity atoms in a semiconductor trend to flow from high concentration to low concentration.
- **Ion Implantation (이온주입)**
  - A process by which ionized atoms are accelerated into a semiconductor substrate through high electrical field.
- **Oxidation (산화)**
  - Oxidation is a process in which a layer of silicon dioxide is thermally grown on a silicon wafer.
- **Lithography (리소그라피)**
  - The lithography process can be divided into two parts: mask making and photoresist operation.
- **Etching (식각) and Cleaning (세척)**
  - A common process is to selectively etch away the layer material not covered by the resist.



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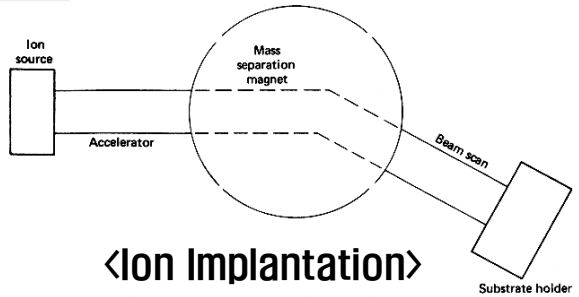
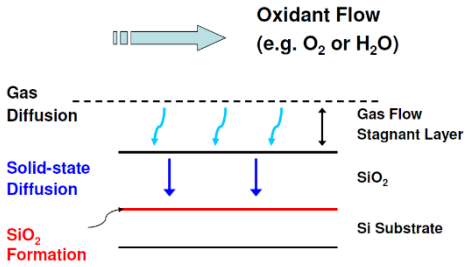
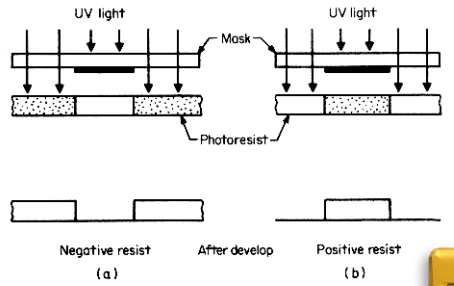


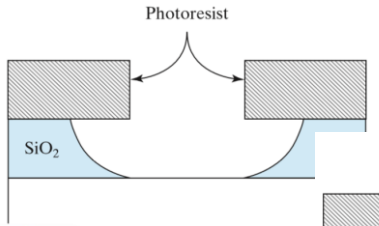
<Ion Implantation>



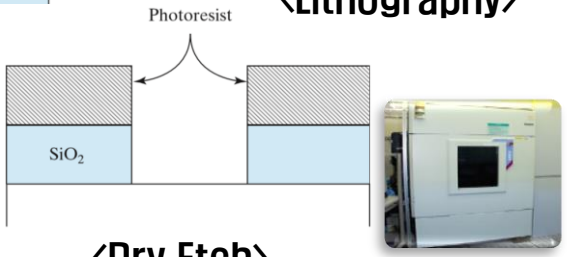
<Oxidation>



<Lithography>

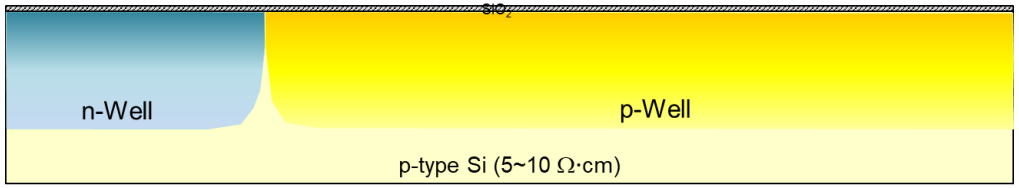



<Wet Etch>

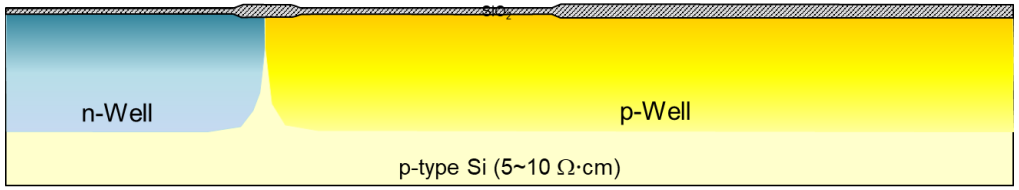


<Dry Etch>

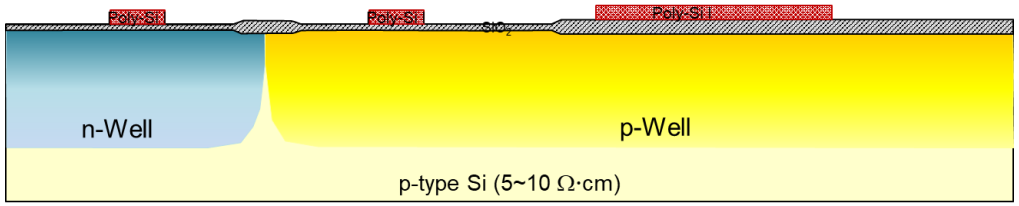
0.5μm Analog CMOS Process Flow



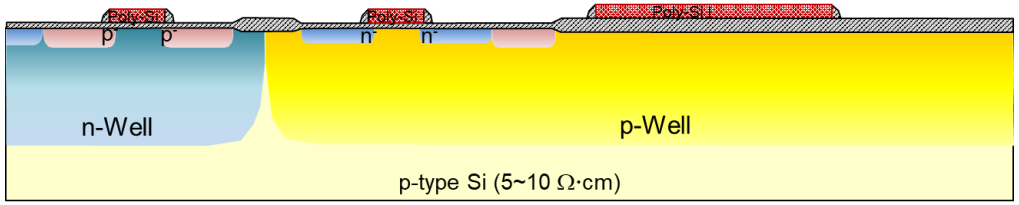
(a) Twin Well Formation



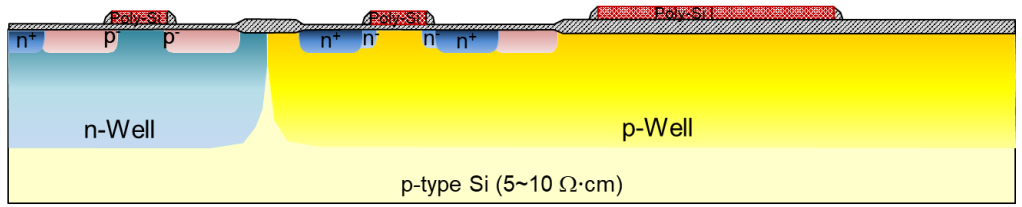
(b) Active Formation



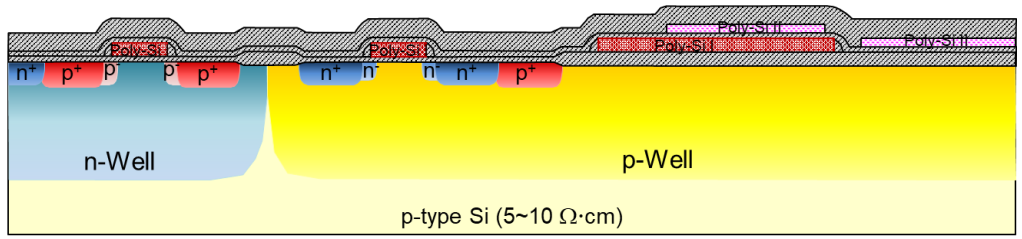
(c) Gate Formation



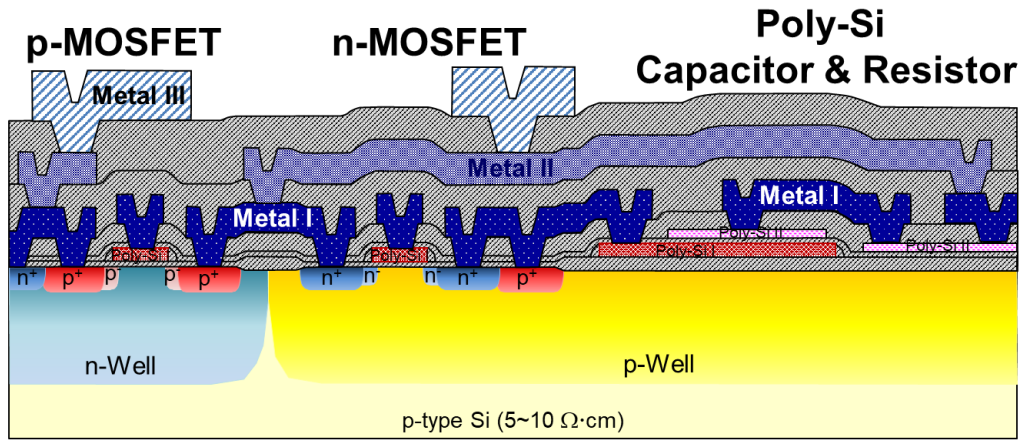
(d) n–LDD and p–LDD Formation



(e) n^+ and p^+ S/D Formation



(f) Passive Device Formation



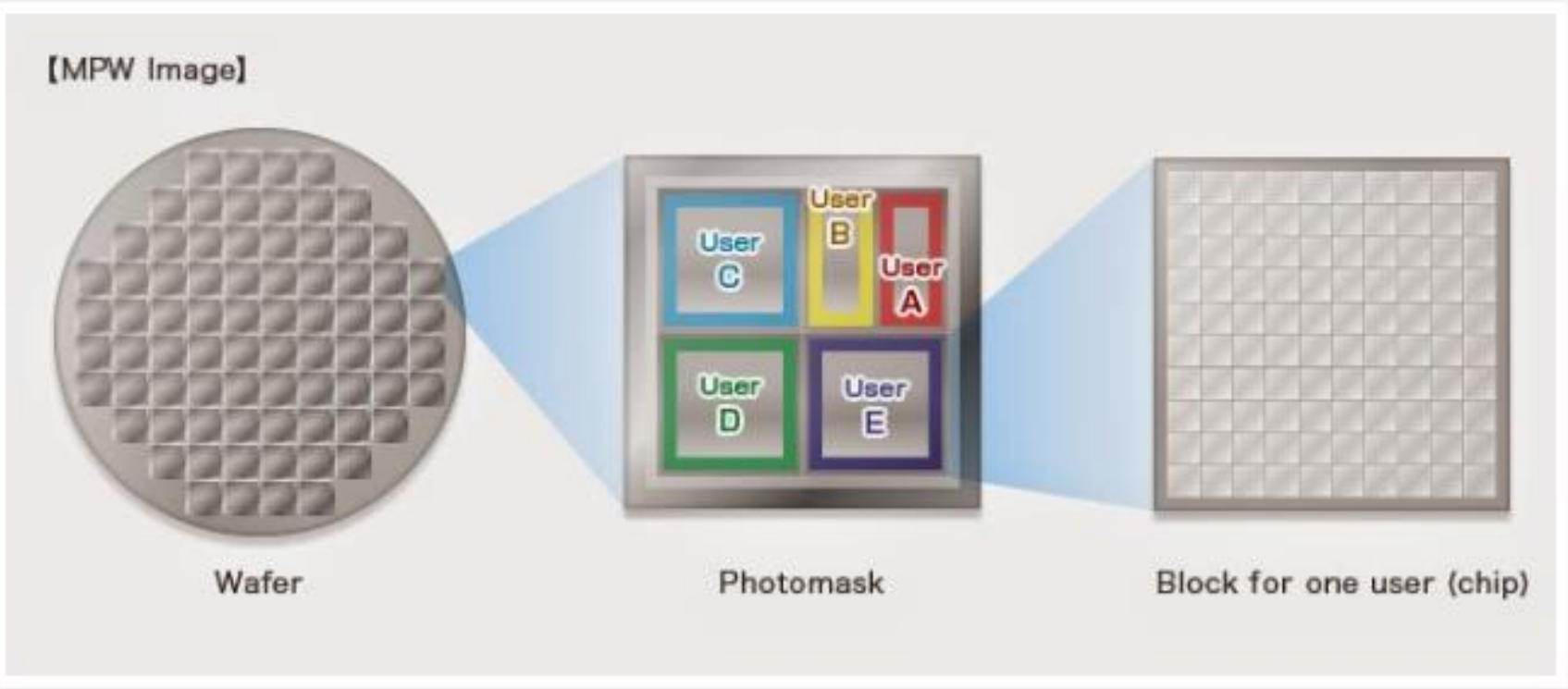
(g) Metallization and Alloy

04. 내 칩(My Chip) 제작 서비스

MPW 개념

- MPW (Multi-Project Wafer)는 설계한 여러 종류의 IC를 한 웨이퍼(Wafer)에 제작하여 요청한 칩을 동시에 의뢰자에게 제공하는 서비스

→ 학생들 본인의 설계 칩을 직접 검증 → 반도체설계 실무 인력 양성



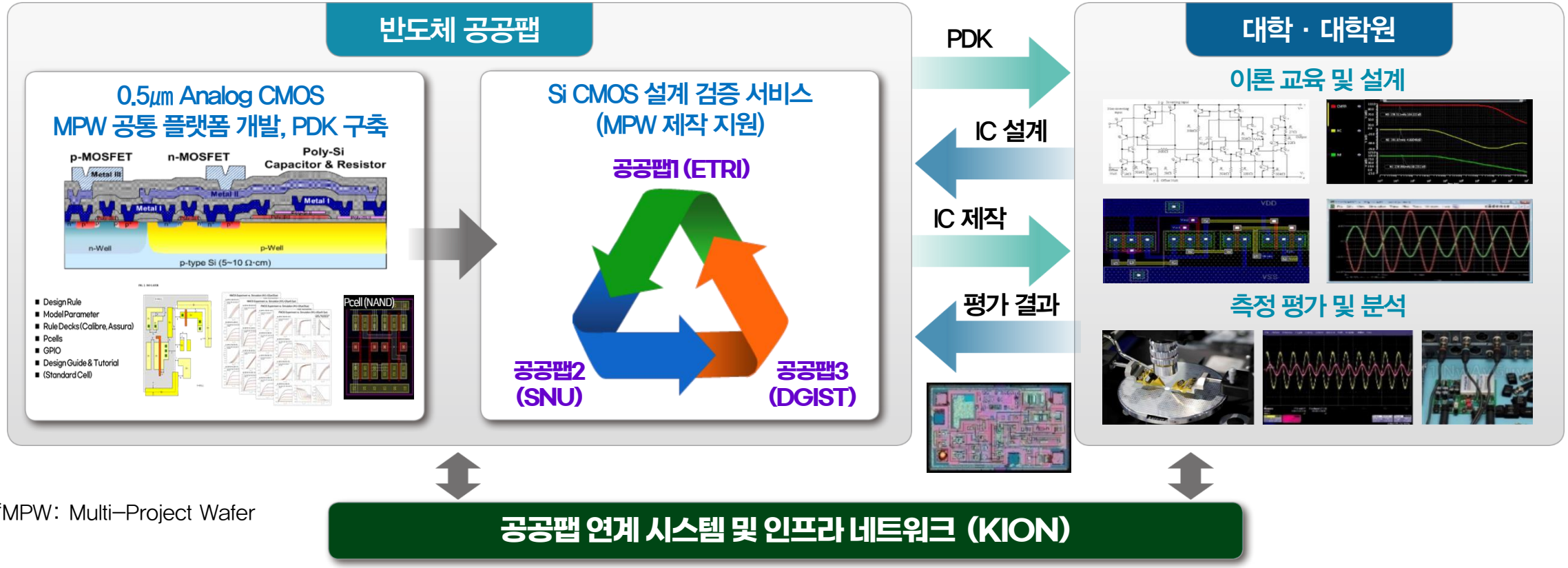
*MPW: Multi-Project Wafer

04. 내 칩(My Chip) 제작 서비스

내 칩(My Chip) 제작 서비스 개념

✓ **반도체 설계 분야의 학부생·대학원생에게 공공팹을 활용한 6인치 CMOS 공정 기반 MPW 제작 지원**

→ 학생들 본인의 설계 칩을 직접 검증 → 반도체설계 실무 인력 양성



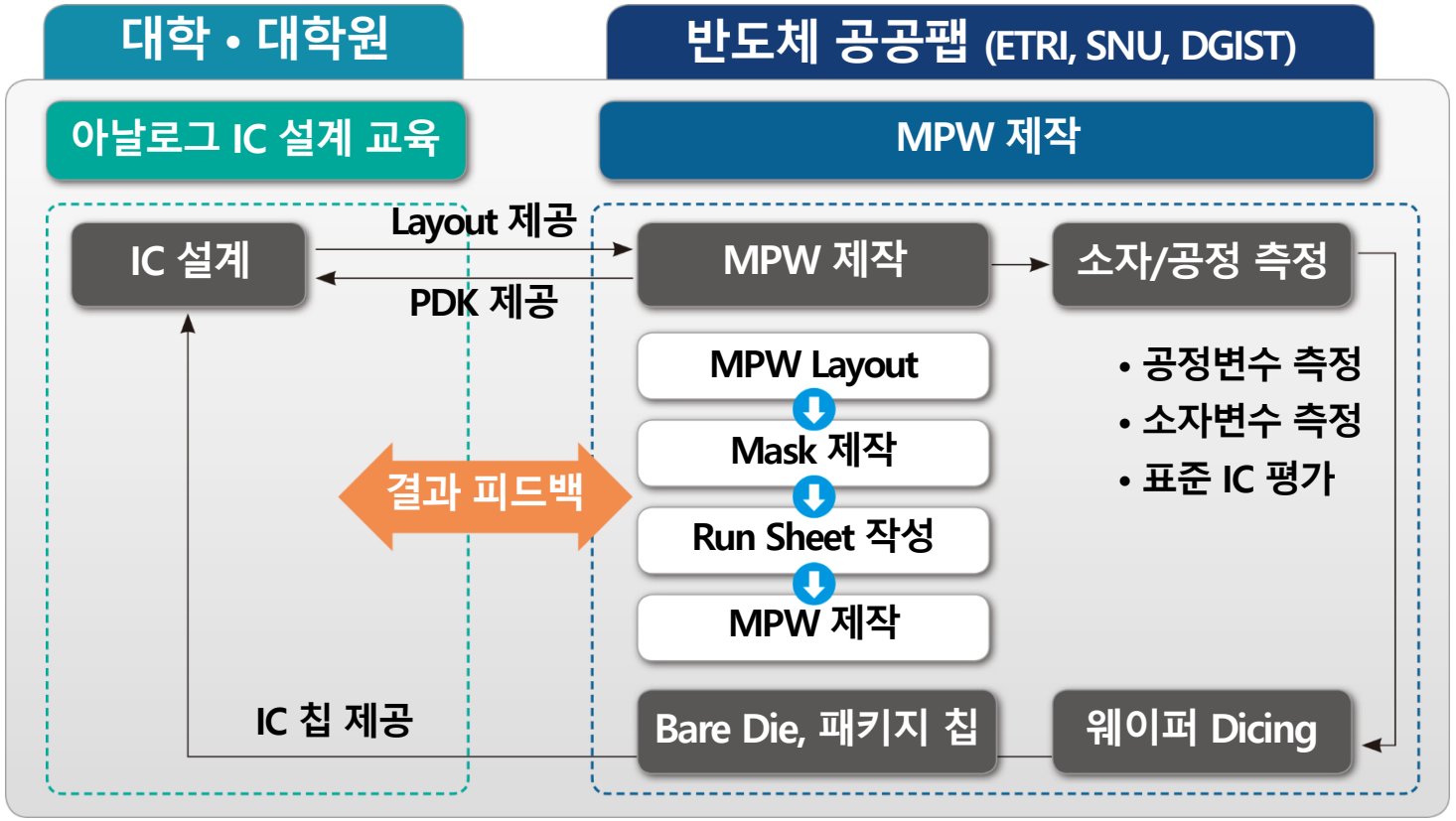
*MPW: Multi-Project Wafer

04. 내 칩(My Chip) 제작 서비스

반도체 설계인력양성을 위한
6인치 Si CMOS 설계검증 플랫폼 개발 및 MPW 지원

내 칩(My Chip) 제작 서비스 지원 개요

MPW 요구 → MPW 요구접수 → PDK 배포 → 설계 DB 수령 → DB 취합/검토 → MPW 제작 → Wafer 검증 → 칩 배포



■**0.5㎛ 아날로그 CMOS IC 설계용 공공팹 공통 PDK 설계 교육기관에 제공**
- PDK 및 디자인 가이드 배포
- 설계자 요구사항 PDK 및 MPW 플랫폼 개발에 반영

■**설계검증용 MPW 칩 제작 지원**
- MPW 1회당 25개 팀(칩) 이상
- 1단계 MPW 연 6회 (1차년도 Test 1회)
- 2단계 MPW 연 12회

■**CMOS 공정 관리를 통한 수율, 균일도 및 재현성 확보**
- 수율 > 70%, 균일도 < 10%
- TAT < 3개월

■**TEG 평가 결과 및 설계검증 칩 제공**

*MPW: Multi-Project Wafer, PDK: Process Design Kit, *DB: Data Base, TEG: Test Element Group, TAT: Turn Around Time

04. 내 칩(My Chip) 제작 서비스

ETRI 한국전자통신연구원

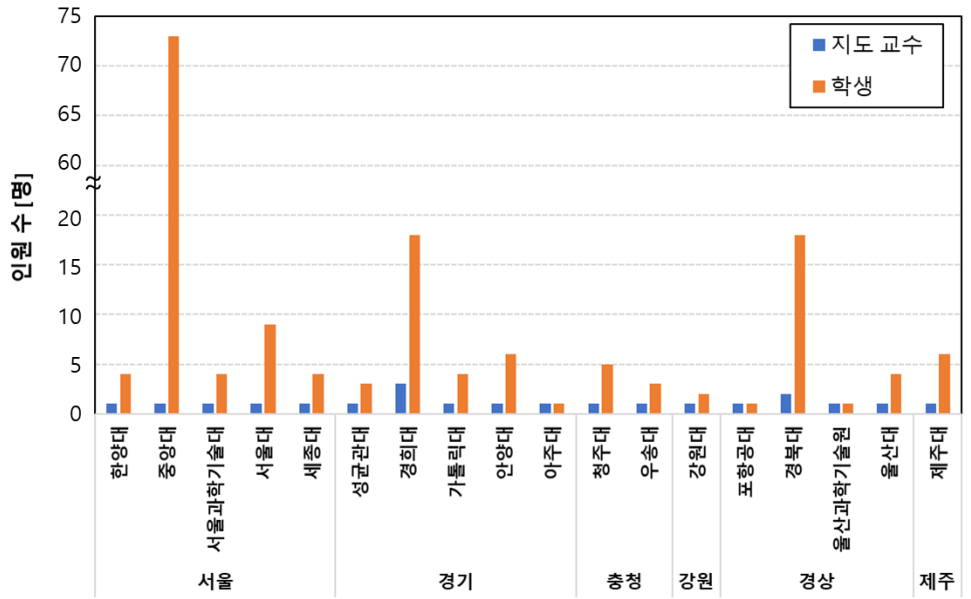
반도체 설계인력양성을 위한
6인치 Si CMOS 설계검증 플랫폼 개발 및 MPW 지원

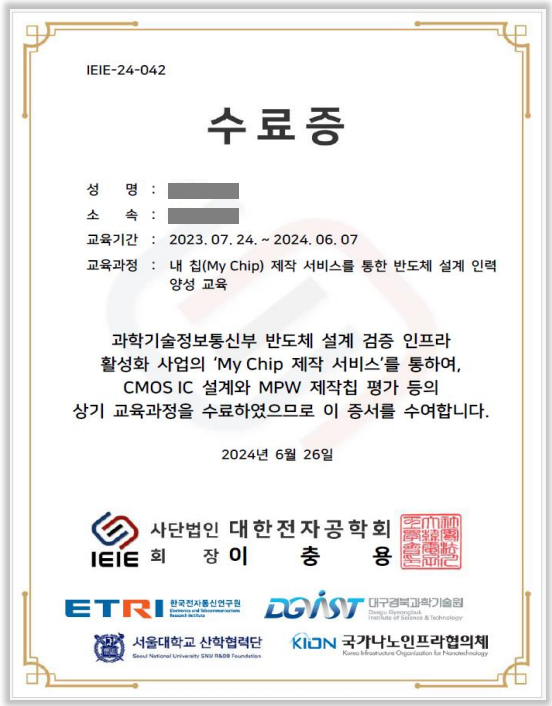
2023년, 시범 "My Chip 제작 서비스"

공고, 신청서 접수 (7/24~8/31)	신청서 평가 (~9/15)	PDK 배포, DB 접수 (9/18~11/17)	Mask, MPW 제작 (11/18~3/26)	패키지, 칩배포 (Bare-Die 4/5, 패키지 5/1)	결과보고서 (~7/31)

- 신청/접수 건수: 설계 DB 접수 25건 → 24건 MPW 제작 (1건 설계 미비)
- 참여 현황: 12개 대학, 지도교수 14명, 참여 팀수 46개 팀 (학생 125명) → MPW Bare-die(4/6) 및 패키지 칩(5/1) 전달
- 결과보고서 접수 35개 팀 (81명) → 34개 팀 (74명) 대한전자공학회 수료증 수여 → 26개 팀(64명) MPW 칩 동작확인

< 대학별 신청현황 >





IEIE-24-042

수 료 증

성 명 : [redacted]
소 속 : [redacted]
교육기간 : 2023. 07. 24. ~ 2024. 06. 07
교육과정 : 내 칩(My Chip) 제작 서비스를 통한 반도체 설계 인력 양성 교육

과학기술정보통신부 반도체 설계 검증 인프라 활성화 사업의 'My Chip 제작 서비스'를 통하여, CMOS IC 설계와 MPW 제작칩 평가 등의 상기 교육과정을 수료하였으므로 이 증서를 수여합니다.

2024년 6월 26일

사단법인 대한전자공학회
IEIE 회 장 이 충 용

ETRI 한국전자통신연구원 DGIST 대구경북과학기술원
서울대학교 산학협력단 KION 국가나노인프라협의체

13

04. 내 칩(My Chip) 제작 서비스

ETRI 한국전자통신연구원

반도체 설계인력양성을 위한
6인치 Si CMOS 설계검증 플랫폼 개발 및 MPW 지원

표준 공정 및 공통 디자인룰

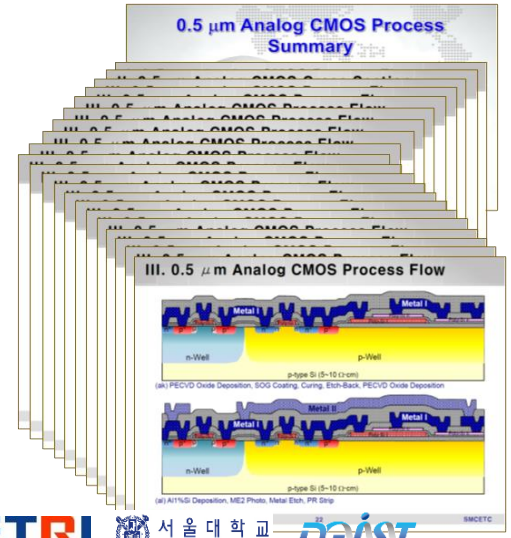
✓ **참여기관간 공정/디자인 협의 → 0.5㎛ Analog CMOS (5V) 표준 공정 및 공통 디자인룰 도출**

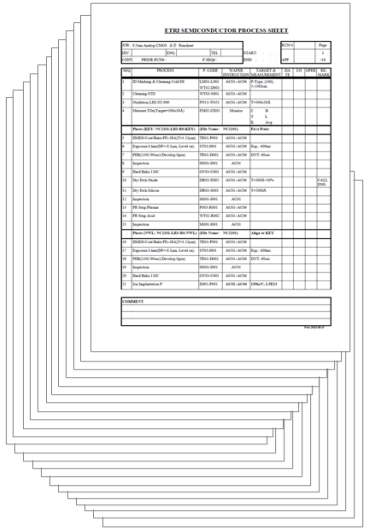
❖ 주요 공정 : 2-Poly, 3-Metal 공정

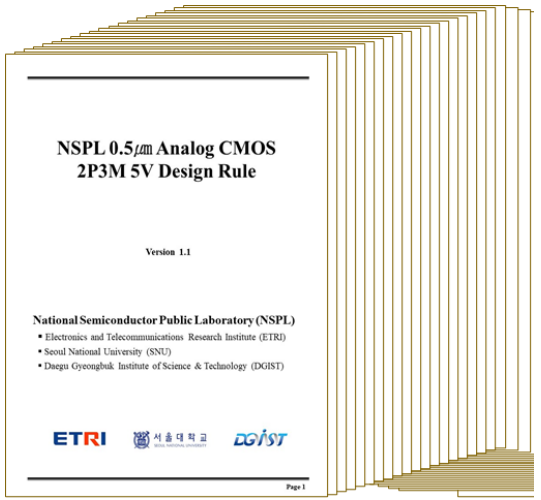
- Diffused Twin Well : 1150℃
- LOCOS Isolation: 950℃, 5200Å
- Gate Oxide = 110Å
- Poly Gate; Undoped Poly + $POCl_3$ Doping (or Doped Poly)
- PIP Capacitor; HTO (or LPCVD-TEOS) 750Å
- Poly2 Resistor; Ph. Implant, ~3.5E15

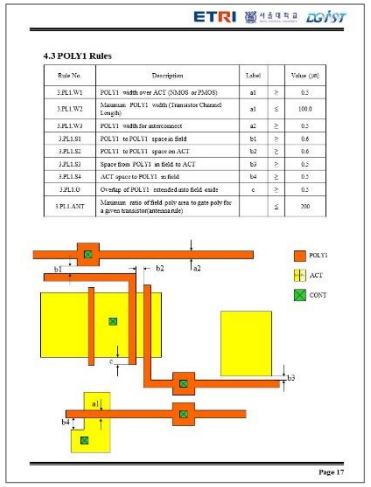
❖ 주요 디자인 룰

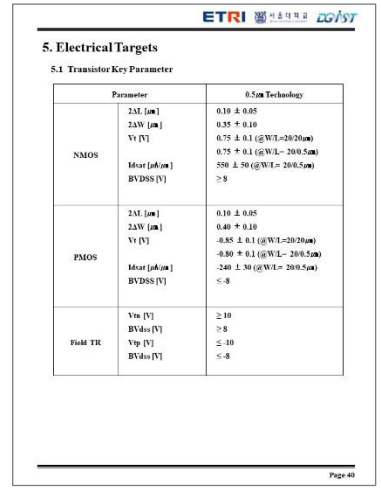
- Minimum Gate (POLY1) Width/Space = 0.5㎛/0.6㎛
- Minimum Active Width/Space = 0.8㎛/0.8㎛
- Minimum Transistor(N/PMOS) width = 1.4㎛
- Minimum Contact Size/Space = 0.6㎛/0.6㎛
- Minimum Via1 & Via2 Size/Space = 0.8㎛/0.8㎛
- Minimum Metal1, 2, 3 Width/Space = 0.8㎛/0.8㎛, 1㎛/1㎛, 1㎛/1㎛











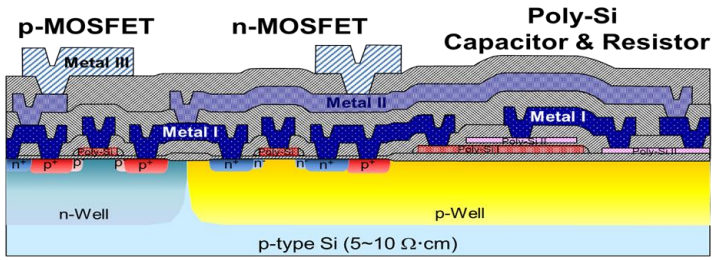
Design Rule

✓ NSPL 0.5㎛ Analog CMOS 2P3M 5V Design Rule

1. Technology Overview

1.1 Process Overview

- 0.5㎛ Analog CMOS (2-poly / 3-Metal)
- Single gate oxide 110Å for 5V CMOS
- Passive components: Poly-Si Resistor/Capacitor



1.2 Process Condition

- N-well lateral diffusion : 1.40㎛ (70%)
- P-well lateral diffusion : 1.40㎛ (70%)
- Field oxide encroachment : 0.15㎛
- Spacer bias : 0.18㎛
- N+ lateral diffusion : 0.16㎛ (80%)
- P+ lateral diffusion : 0.20㎛ (80%)

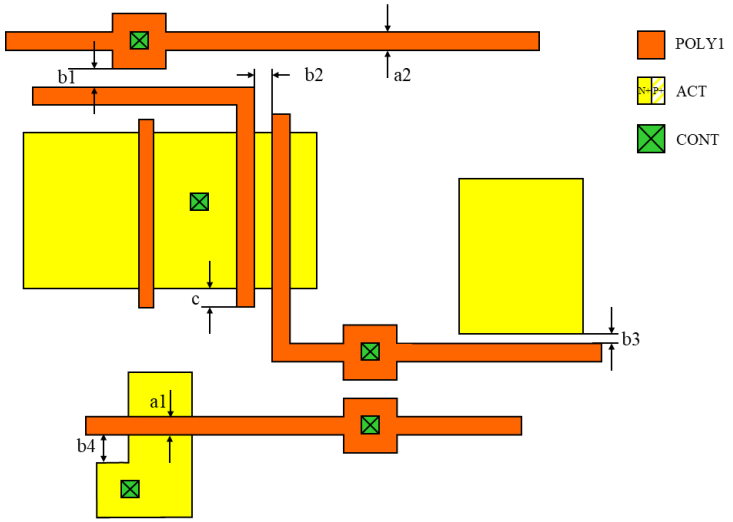
1.3 Align Tolerance

1) Direct alignment
- Critical layers : ±0.15㎛
- Noncritical layers : ±0.20㎛

2) Indirect alignment
: $[X12^2 + X23^2 + \cdots\cdots Xn(n+1)^2]^{0.5}$
Where Xim is the direct alignment tolerance between layer i and m.

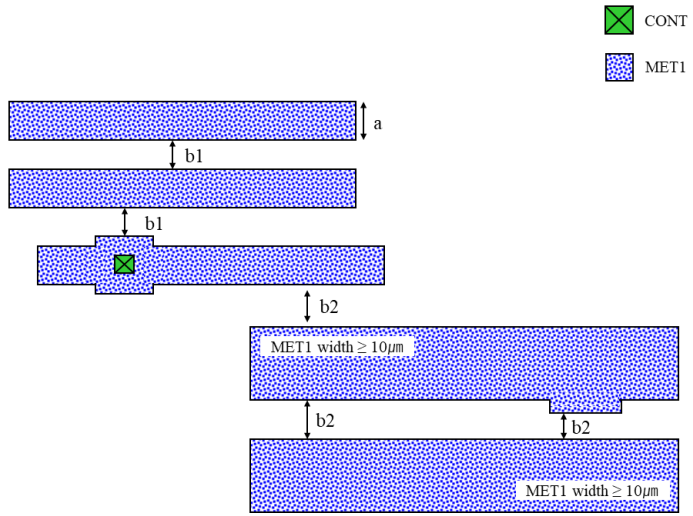
4.3 POLY1 Rules

Rule No.	Description	Label		Value (㎛)
3.PL1.W1	POLY1 width over ACT (NMOS or PMOS)	a1	≥	0.5
3.PL1.W2	Maximum POLY1 width (Transistor Channel Length)	a1	≤	100.0
3.PL1.W3	POLY1 width for interconnect	a2	≥	0.5
3.PL1.S1	POLY1 to POLY1 space in field	b1	≥	0.6
3.PL1.S2	POLY1 to POLY1 space on ACT	b2	≥	0.6
3.PL1.S3	Space from POLY1 in field to ACT	b3	≥	0.5
3.PL1.S4	ACT space to POLY1 in field	b4	≥	0.5
3.PL1.O	Overlap of POLY1 extended into field oxide	c	≥	0.5
3.PL1.ANT	Maximum ratio of field poly area to gate poly for a given transistor(antenna rule)		≤	200



4.8 MET1 Rules

Rule No.	Description	Label		Value (㎛)
8.MET1.W	Width	a	≥	0.8
8.MET1.S1	Space of MET1 (both MET1 width < 10㎛)	b1	≥	0.8
8.MET1.S2	Space of wide MET1 (one or both MET1 width ≥ 10㎛)	b2	≥	1.0
8.MET1.ANT	Maximum ratio of MET1 area to associated gate poly area for a given transistor(antenna rule)		≤	400



Design Guide

✓ NSPL 0.5㎛ Analog CMOS 2P3M 5V Design Guide

1. Overview

1.1 Overview

The purpose of this guide is NSPL 0.5um Analog CMOS 2P3M 5V Design guide.

1.2 Software Version and Tools

- Virtuoso 6.1.8 version
- Calibre 2019.3_15.11

1.3 File Configuration

File : NSPL_0p5um_Analog_CMO

- NSPL_0p5um_Analog_CMOS_2P3M
  - NSPL_0p5um_Analog_CMOS_2P
  - NSPL_0p5um_Analog_CMOS_2P
  - display.drf
  - NSPL_0p5um_Analog_CMOS_2P
  - NSPL_0p5um_Analog_CMOS_2P
  - NSPL_0p5um_Analog_CMOS_2P
  - NSPL_0p5um_Analog_CMOS_2P
  - Calibre/DRC
    - NSPL_0p5um_Analog_CMOS
    - drc_header.cal , rundrc.com
  - Calibre/ LVS
    - NSPL_0p5um_Analog_CMOS
    - lvs_header.cal , runlvs.com
  - Calibre/LVL
    - NSPL_0p5um_Analog_CMOS
    - lvl_header.cal . runlvl.com
  - Calibre/PEX
    - NSPL_0p5um_Analog_CMOS
    - pex_header.cal
    - LPE_LIB : LPE L
  - Assura/DRC
    - NSPL_0p5um_Analog_CMOS_2P3M_5V_DRC.rul : drc rul
  - Assura/LVS
    - NSPL_0p5um_Analog_CMOS_2P3M_5V_LVS_compare.rul : lvs
    - NSPL_0p5um_Analog_CMOS_2P3M_5V_LVS_extract.rul : lvs

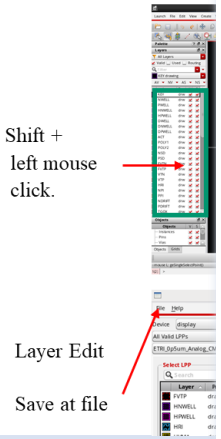
1.4 Documents

- NSPL 0.5um Analog CMOS 2P3M 5V Design Rule
- NSPL 0.5um Analog CMOS 2P3M 5V Design Guide

2. Environment Files and About Use

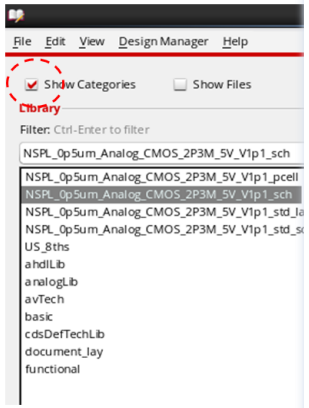
2.1 Display.drf File

- This file should exist in th
- This file the color of the la
- If you want to change the

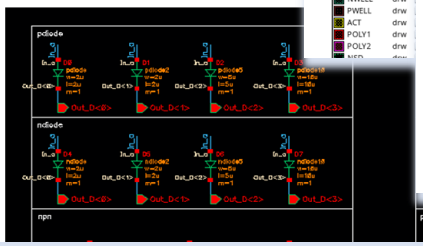


3. Schematic Library

3.1 Library Category

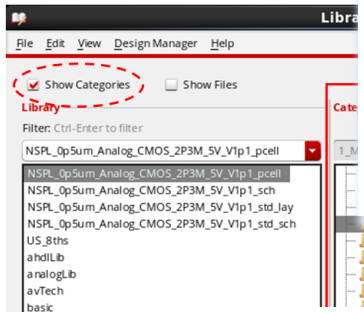


3.2 .Device_ALL



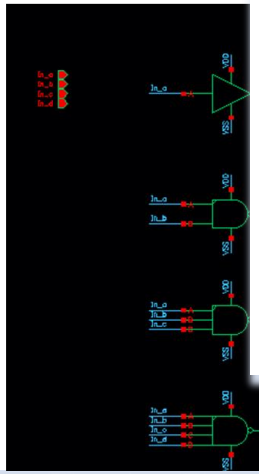
4. PCELL Layout Library

4.1 Library Category

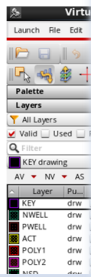


5. Standard Schematic Library

5.1 .SAMPLE

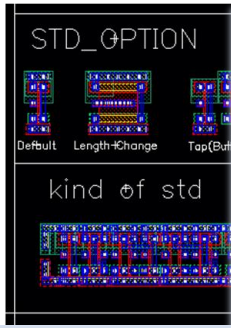


4.2 .Dev



6. Standard Layout Library

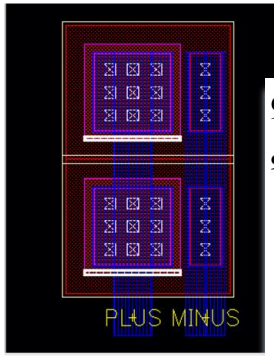
6.1 .SAMPLE



8. LVS Guide

8.1 PIPCAP Layout/Circuit Structure

- Case1 : Merged PIPCAP



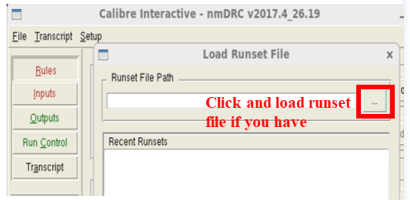
9. Calibre DRC

9.1 Run for DRC at GUI

- For running DRC(Design Rule Check) at GUI after layout, need to several steps like below pictures

1 Click Run nmDRC in Calibre menu

2 If runset file is exist, Load runset file. Runset file is not exist, click cancel



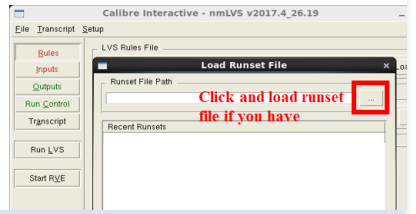
10. Calibre LVS

10.1 Run for LVS at GUI

- For running LVS(Layout VS Schematic) at GUI after layout, need to several steps like below pictures

1 Click Run nmLVS in Calibre menu

2 If runset file is exist, Load runset file. Runset file is not exist, click cancel



04. 내 칩(My Chip) 제작 서비스

ETRI 한국전자통신연구원

반도체 설계인력양성을 위한
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Design Tutorial

✓ 0.5um Analog CMOS 2P3M 5V Design Tutorial

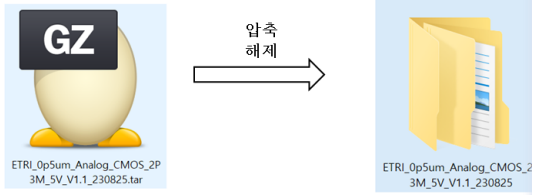
2. PDK Library 설정

- 목적 : 회로 설계 및 검증에 앞서 제공받은 PDK를 설정

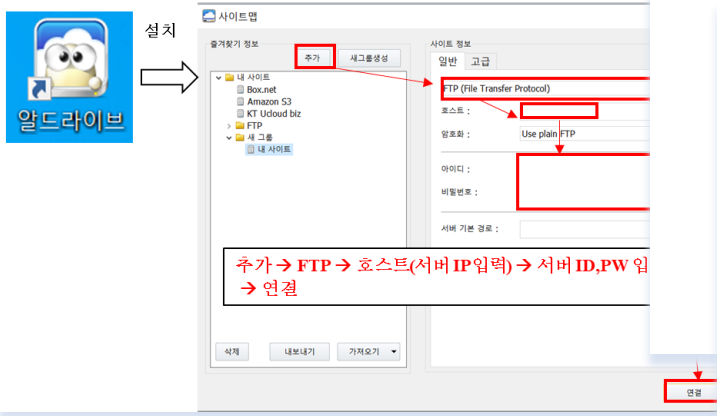
1) PDK Library 전송 (서버 기반의 워크스테이션 접속일 경우)

- 제공된 PDK를 FTP(File Transfer Protocol)을 이용하여 워크스

① 제공된 PDK 파일 압축 해제



② FTP 프로그램 설치 및 설정 (예시로 알드라이브 사용)

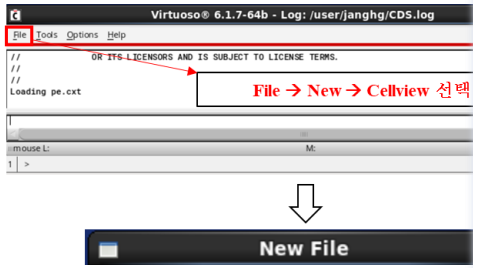


3. 회로 설계 및 검증(Pre-simulation)

- 목적 : 회로 설계 및 시뮬레이션을 통한 회로 검증
- 예: 인버터 회로 설계 및 검증

1) 인버터 설계

① Schematic 설계 프로그램 실행

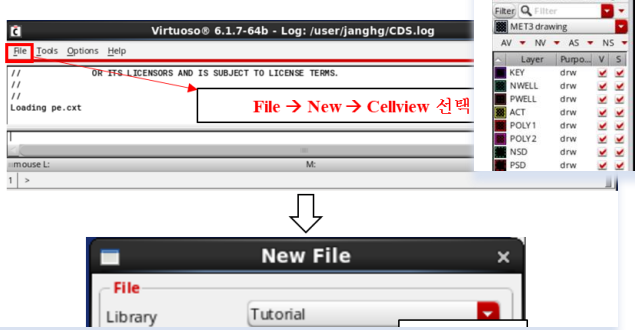


4. Layout

- 목적 : 반도체 회로 제작을 위한 레이아웃 설계
- 예: 설계된 인버터 회로 적용

1) 인버터 회로의 레이아웃 설계

① 레이아웃 디자인 설계 프로그램 실행

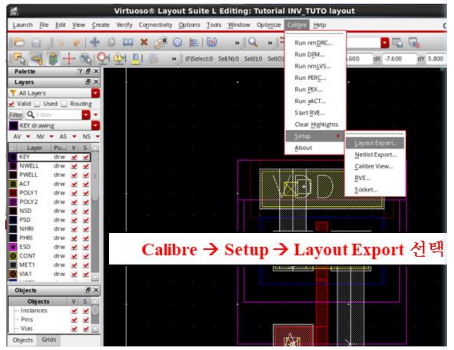


5. DRC

- 목적 : 설계된 레이아웃 디자인이 디자인룰에 적합한지 검토

1) Calibre DRC 검토

① DRC 검증 방법

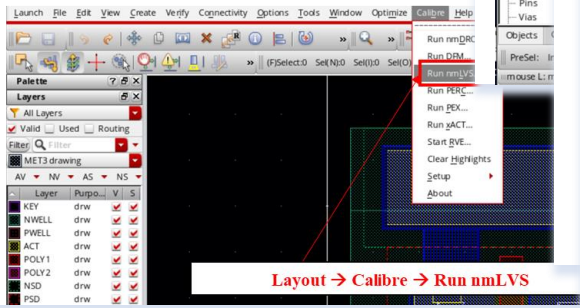


6. LVS

- 목적 : 설계한 Layout과 Schematic 비교

1) Calibre LVS 검토

① LVS 검증 방법

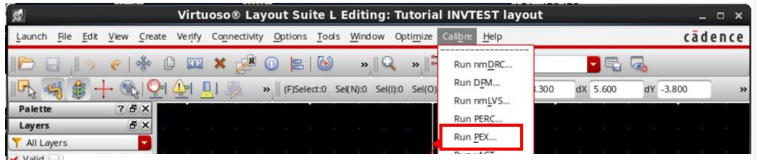


7. PEX

- 목적 : Parasitic 성분 추출

1) Calibre PEX 검토

① PEX 진행 방법

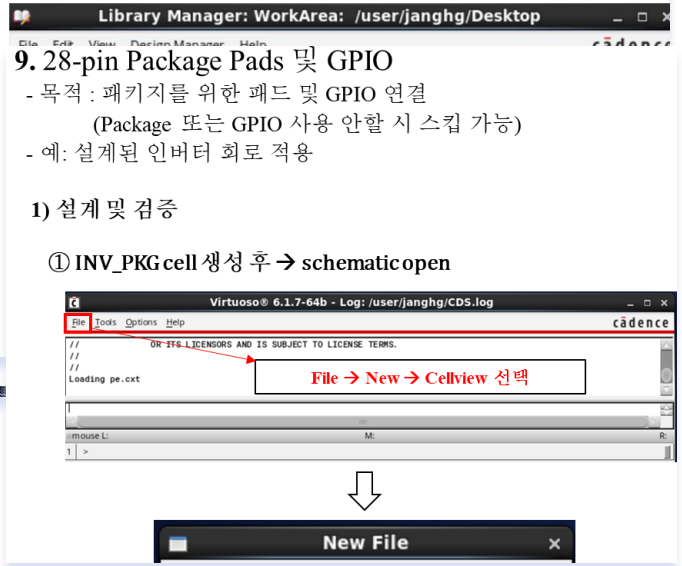


8. 회로 설계 및 검증 (Post-simulation)

- 목적 : Parasitic 성분 반영한 시뮬레이션을 통해 Pre-sim.과 결과 비교

1) Post-simulation

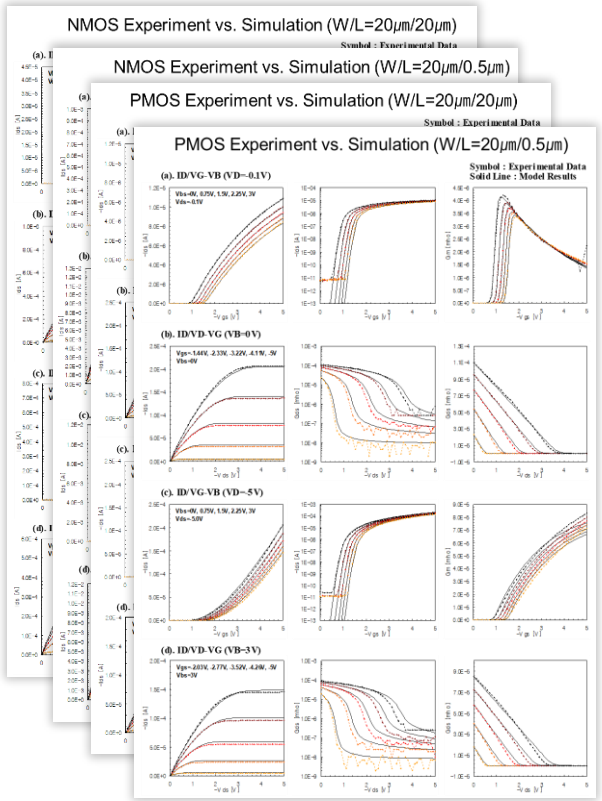
① Schematic 설계 프로그램 실행

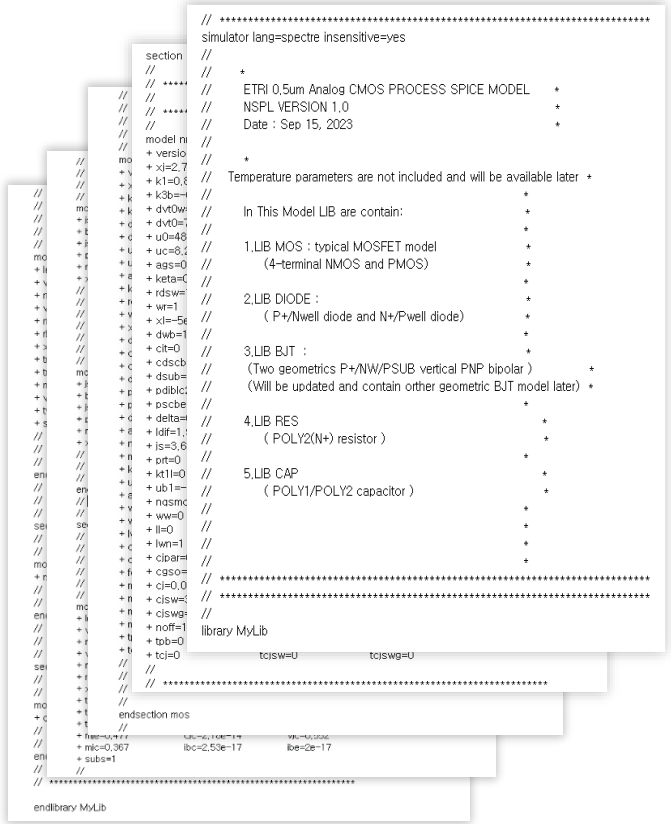


ETRI 서울대학교 SEOUL NATIONAL UNIVERSITY DGIST

PDK (Process Design Kit)

- Design Rule
- Model Parameter
- Rule Decks (Calibre, Assura)
- Pcells
- GPIO
- Design Guide & Tutorial
- (Standard Cell)





(1) Model Parameter

- ✓ Devices: CMOS, Sub-BJT, Diode, Resistor, Capacitor
- ✓ DC Parameter
- ✓ Capacitance Parameter
- ✓ Temperature Parameter
- ✓ Corner Model (MOSFET)
- ✓ (미제공) RF Parameter, Noise Parameter

ETRI 한국전자통신연구원

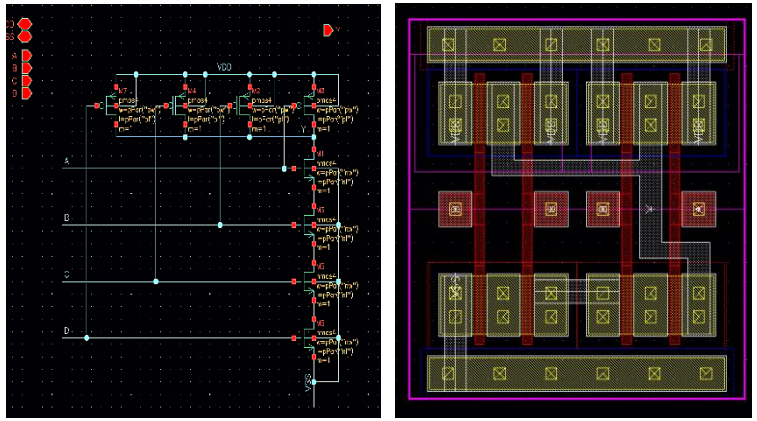
반도체 설계인력양성을 위한
6인치 Si CMOS 설계검증 플랫폼 개발 및 MPW 지원

PDK (Process Design Kit)

(2) Rule Decks, Pcells, Standard Cell

- ✓ Calibre, Assura: DRC, LVS, PEX, Antenna Rule
- ✓ Pcell: CMOS, BJT, Diode, Cap, Res, Logic Gate 등
- ✓ Digital IC 설계용 Standard Cell 구축 예정 (`25년 ~ `26년)

〈Pcell 예: nand4〉



〈MOSIS 제공 Standard Cell〉

The IIT cell library has been developed to provide a free, non-proprietary library for MOSIS SCMOS rules.

It supports both commercial and public domain EDA tools.

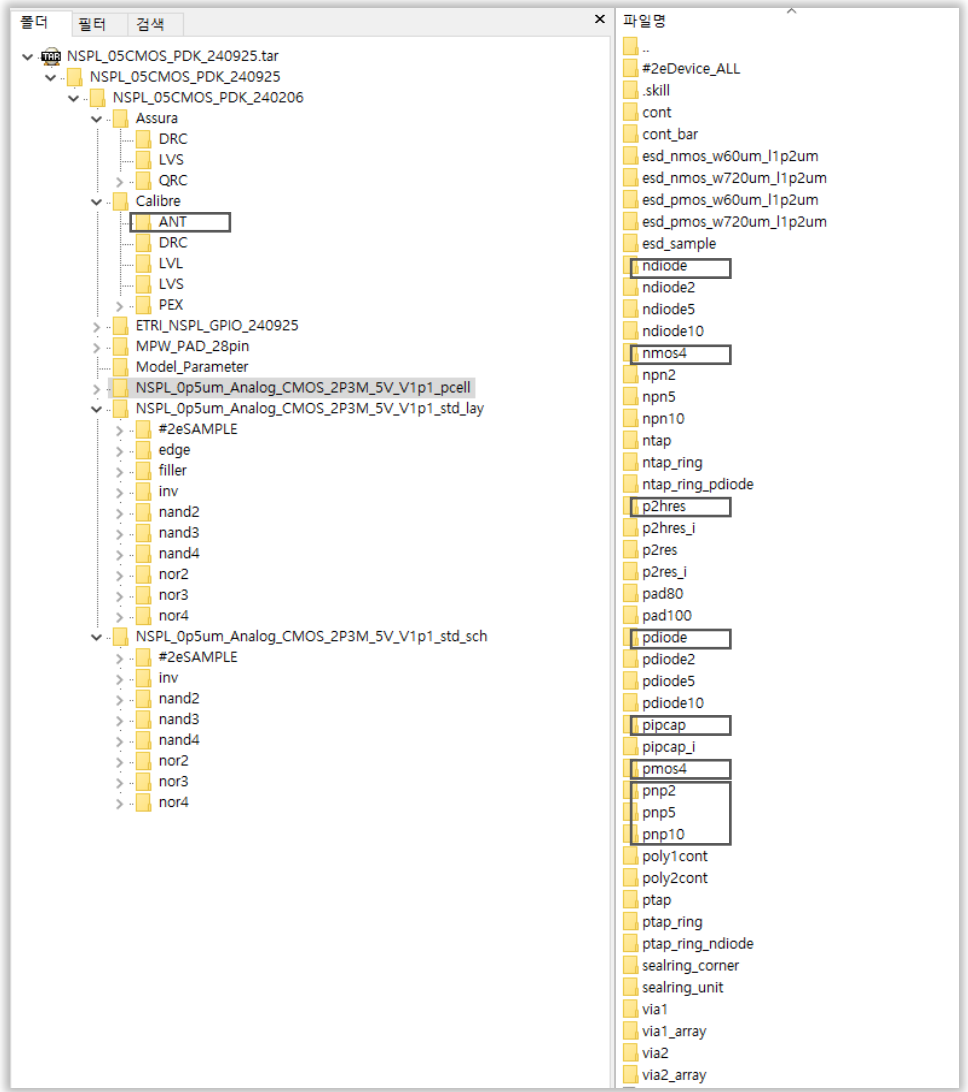
The library is available for free upon request from http://vlsi.ece.iit.edu/scells

List of Cells

AND2X1	INVX4
AND2X2	INVX8
AOI21X1	LATCH
AOI22X1	MUX2X1
BUFX2	NAND2X1
BUFX4	NAND3X1
CLKBUF1	NOR2X1
CLKBUF2	NOR3X1
CLKBUF3	OAI21X1
DFFNEGX1	OAI22X1
DFFPOSX1	OR2X1
DFFSR	OR2X2
FAX1	TBUFX1
FILL	TBUFX2
HAX1	XNOR2X1
INVX1	XOR2X1
INVX2	

Supported MOSIS Technologies

- AMI 0.5µm (includes pads)
- AMI 0.35µm (includes pads)
- TSMC 0.25µm
- TSMC 0.18µm

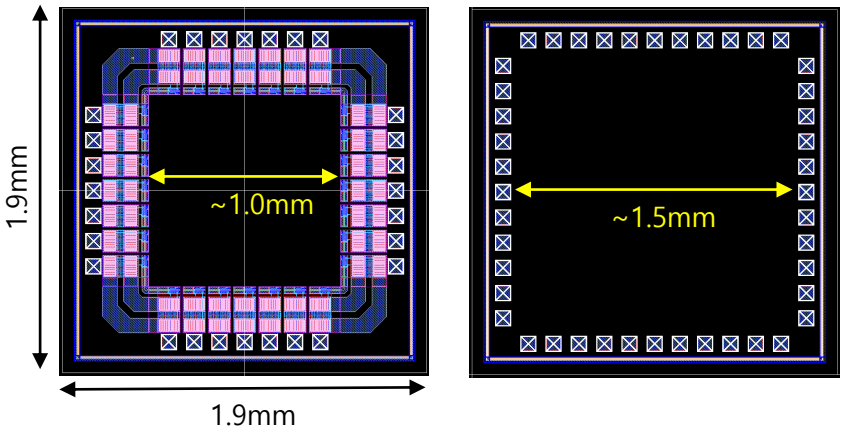


PDK (Process Design Kit)

(3) GPIO (general-purpose input/output), 표준 PAD

✔ 공공팹 공통 디자인룰 기반 Analog/Digital IC용 IO 9종

No.	Name	Function	Schematic	Layout
1	PIC	Input Cell		
2	POB4	Output Cell with 4mA Driving Ability		
3	POB8	Output Cell with 8mA Driving Ability		
4	POB24	Output Cell with 24mA Driving Ability		
5	PBCT4	Bi directional Cell with 4mA Driving Ability, CMOS Input		
6	PBCT8	Bi directional Cell with 8mA Driving Ability, CMOS Input		
7	PANA	Analog Cell(N/P Diode Size : 30umx30umx4)		
8	PVDD	Power Clamp Cell		
9	PVSS	Ground Clamp Cell		

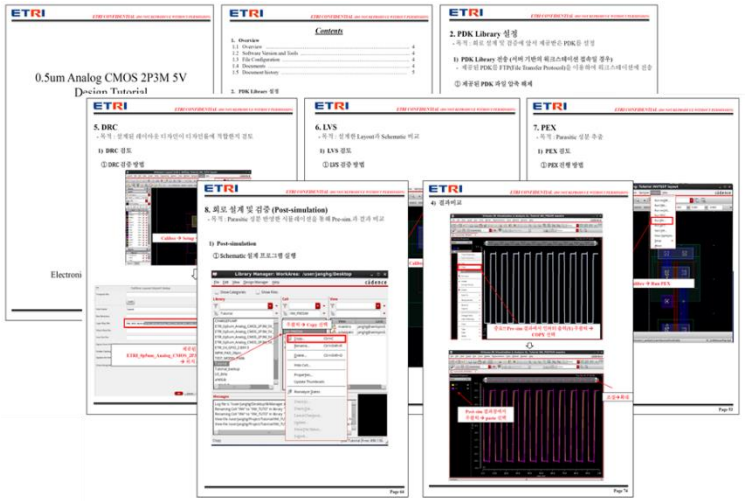


<GPIO사용 및 패키지 진행 경우> <패키지 미진행 → PAD 임의 배치>

(4) Design Guide 및 Tutorial

✔ Design Guide
: PDK 환경 설정, Schematic, Pcell 및 Standard Cell 사용 지침서

✔ Design Tutorial
: Circuit Simulation, Layout, DRC/LVS/PEX 등 설계 실무 지도서



04. 내 칩(My Chip) 제작 서비스

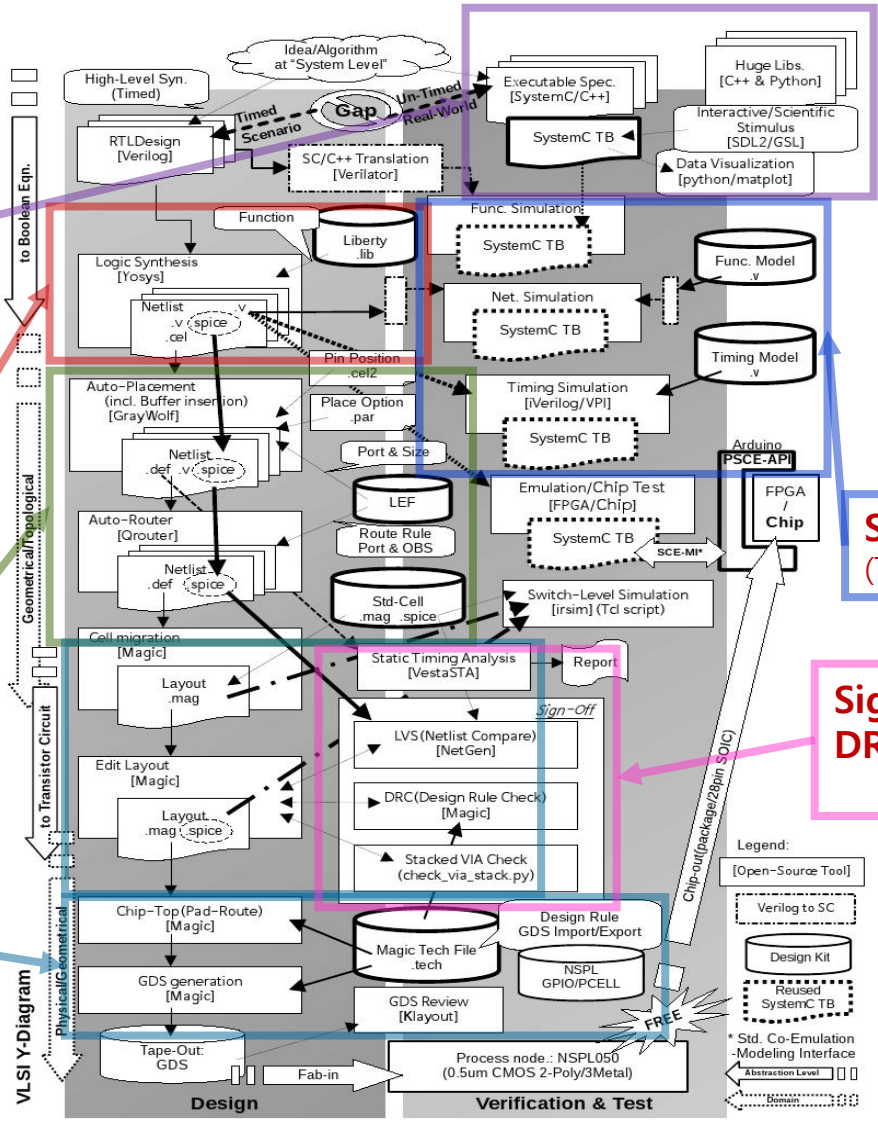
오픈소스 디지털 설계 Flow

0.5㎛ CMOS 기반 오픈소스 디지털 설계 Flow 완성 - My Chip 칩 설계 및 제작 성공 !!!

표 1. 디자인 킷에 활용된 오픈 소스 도구 및 라이브러리 목록

도구 명	용도
SystemC[9]	시스템 수준 모델링 C++ 크래스 라이브러리
GSL[10]	C/C++ 과학 라이브러리 (GNU Scientific Library) 시뮬레이션 데이터 생성 및 분석
SDL2[11]	멀티미디어 C/C++ 라이브러리 (Simple Directmedia Layer). 대화형 테스트 벤치
python[12]	시뮬레이션 데이터 분석 및 시각화
iVerilog[13]	베릴로그 시뮬레이터
irsim[16]	스위치 레벨 시뮬레이터
ngSpice[15]	SPICE 회로 시뮬레이터
XSchem[18]	회로도 작성
Verilator[19]	베릴로그-C++ 변환기
Yosys[20]	RTL 베릴로그 합성기 **Liberty**
GrayWolf[22]	자동 배치 배선기. 버퍼 삽입 기능 포함 **LEF**
Qrouter[23]	자동 배선기 **(Routing Dule/DRC, Obstruction)**
Magic[24]	레이아웃 편집, DRC, GDS 생성 **Magic Tech**
NetGen[25]	네트리스트 비교 방식 LVS **(DRC)**
QFlow[26]	설계 플로우 관리 도구

디자인 킷 배포 링크: https://github.com/GoodKook/ETRI-0.5um-CMOS-MPW-Std-Cell-DK
문의: 국일호/공학박사 goodkook@gmail.com



Simulation Verilog Model
(Testbench Reuse/VPI)

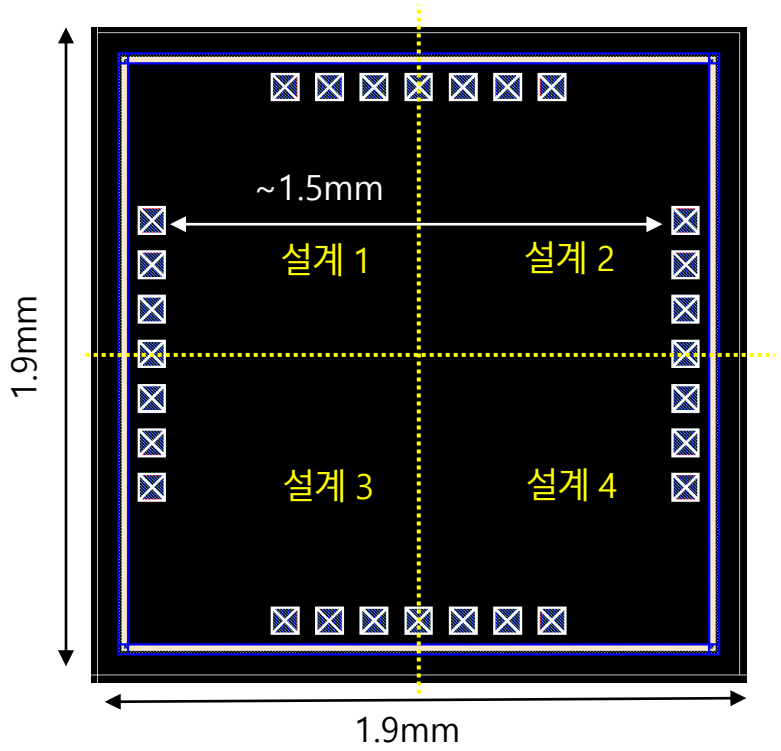
Sign-Off:
DRC, LVS, Stacked VIA
(Tcl, python)

04. 내 칩(My Chip) 제작 서비스

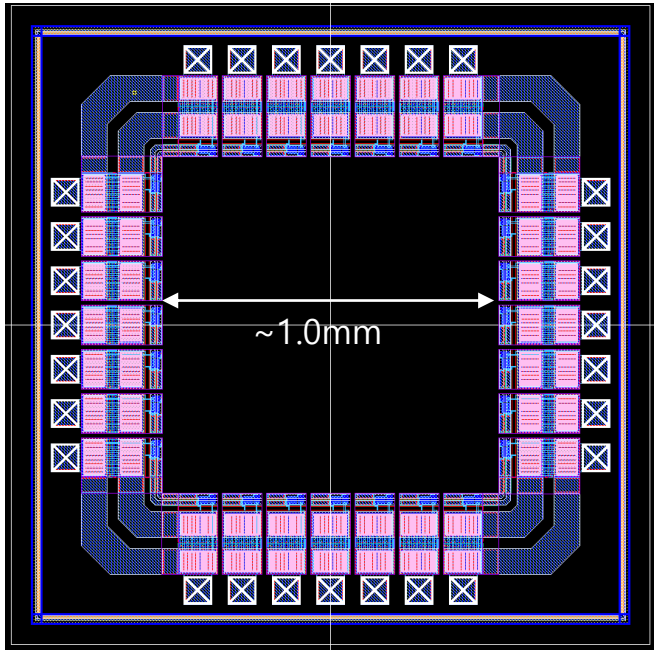
MPW 칩 구성

- ✓ Chip size : 1.9mm x 1.9mm, 1팀당 설계 면적 1.5mm x 1.5mm 활용, GPIO 사용시 설계 면적 1.0mm x 1.0mm 활용
- ✓ 팀(칩)당 구성인원 제한은 없으나 4명 내외 구성 권장
- ✓ 칩 크기가 다를 경우 별도 협의

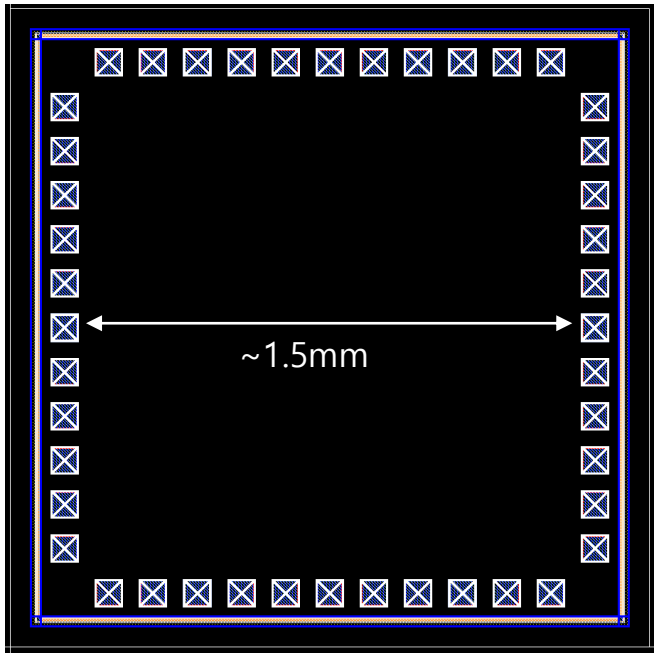
▣ **PAD 기본 정보**



▣ **GPIO사용 및 패키지 진행 경우 (예)**



▣ **패키지 진행하지 않는 경우 (예)**
→ PAD 자유로이 배치

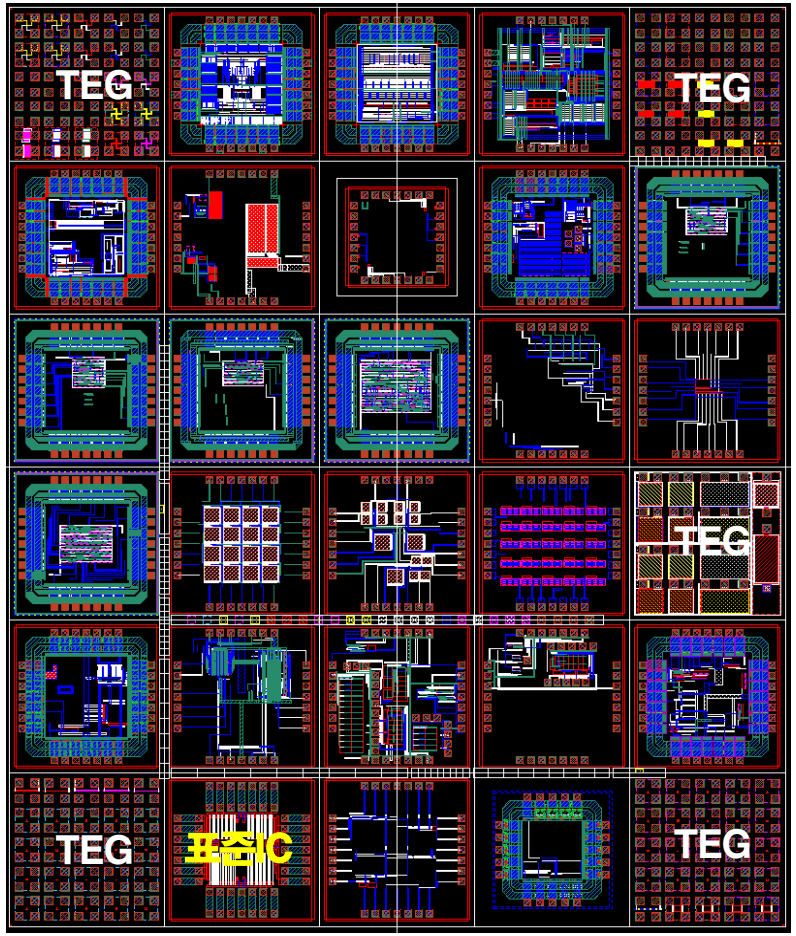


04. 내 칩(My Chip) 제작 서비스

ETRI 한국전자통신연구원

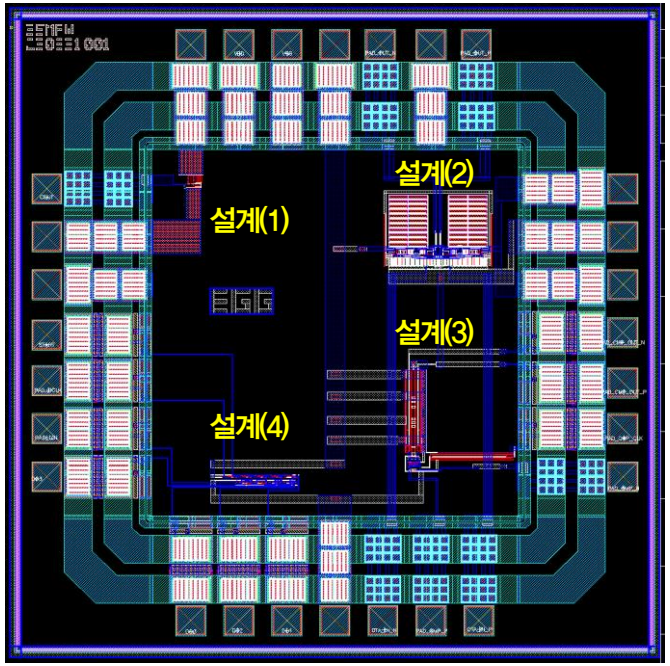
MPW 현황

설계 DB 취합



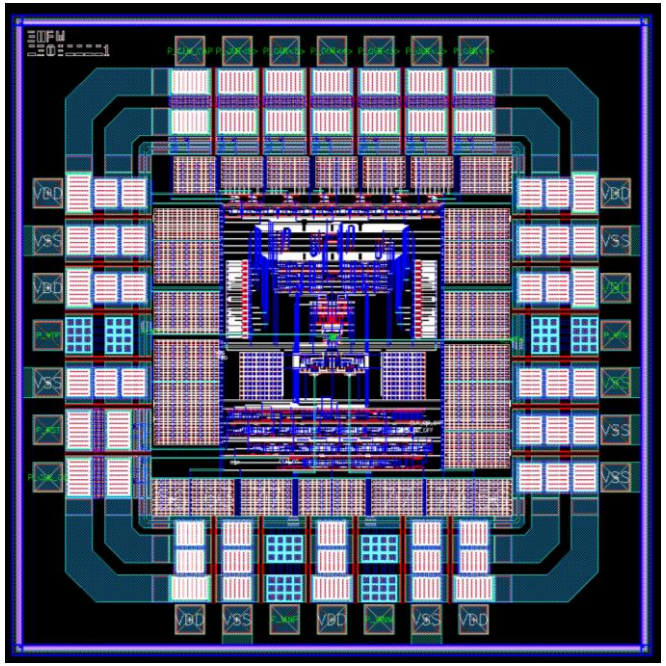
설계 예(1): 팀원 각자 본인 칩 설계

- 설계명: (1) 80dB-100MHz fully differential amplifier, (2) 100uA current reference, (3) 4-bit SIPO shift register, (4) StrongARM latch
- 팀수(학생수): 1팀(4명), 학부4학년



설계 예(2): 팀원 협력하여 1칩 설계

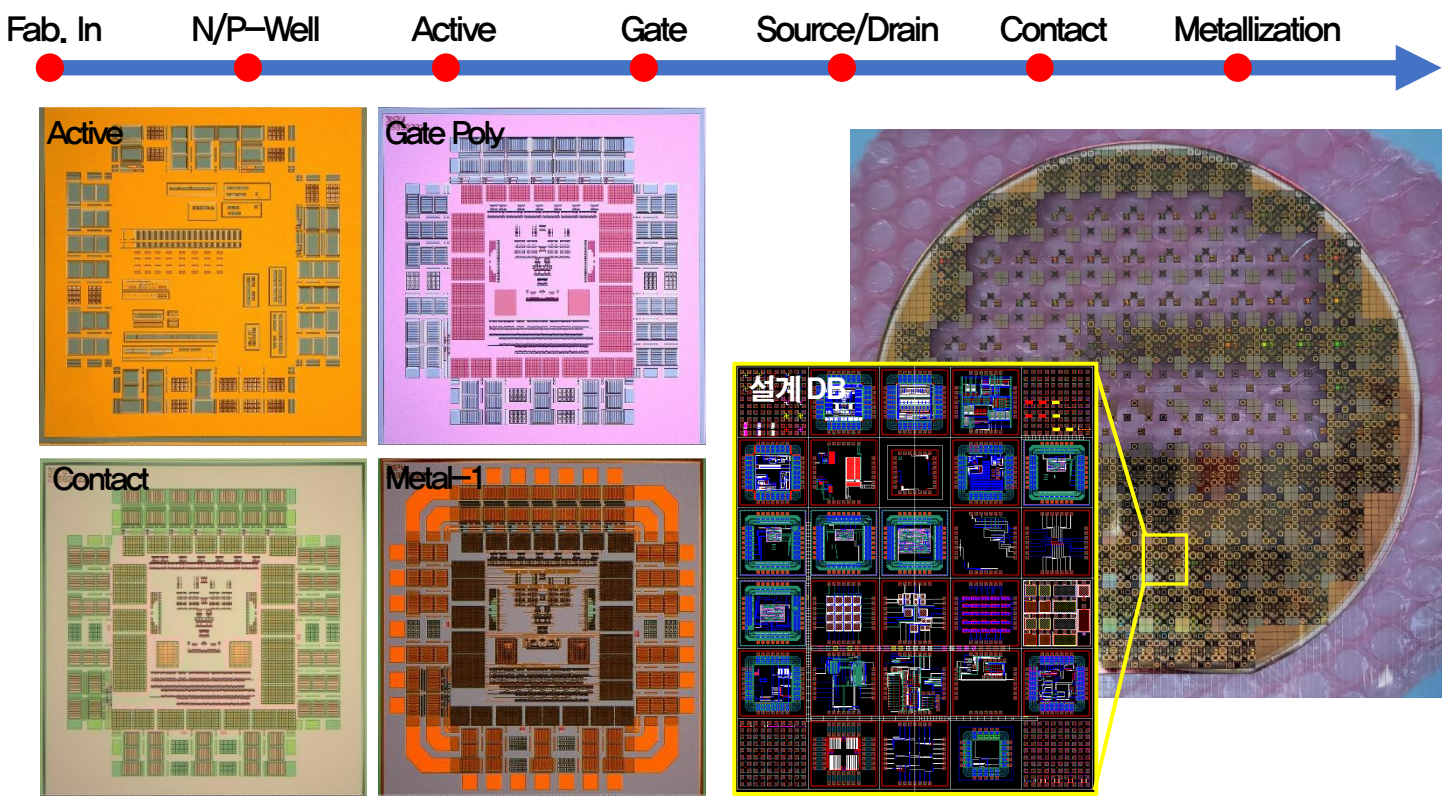
- 설계명: 상보 증폭기를 이용한 고속 데이터 변환기 개발 (A 2-times time-domain interpolating Flash ADC with complementary dynamic amplifier)
- 팀수(학생수): 1팀(3명), 학부4학년



04. 내 칩(My Chip) 제작 서비스

MPW 제작 및 칩 패키지

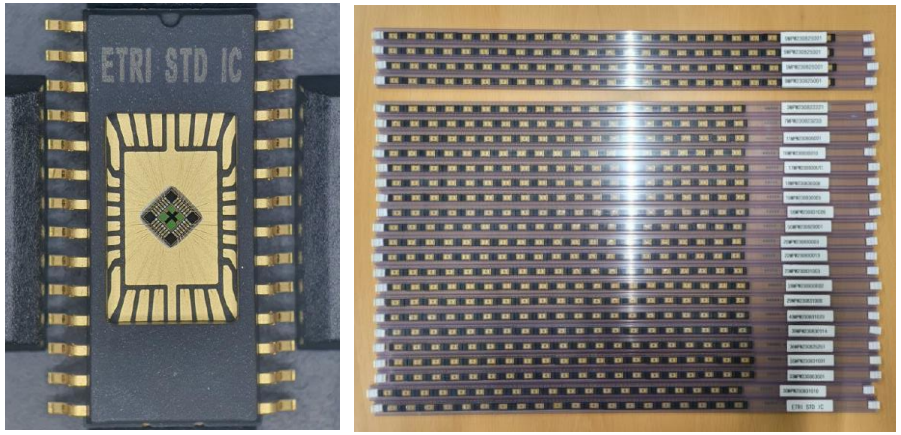
- 0.5㎛ CMOS (2-Poly/3-Metal) 공정으로 24개 칩에 대한 MPW 제작 (총 20 Photolithography, ~230 공정 Step)
- 팀당 Bare-Die 30개, 패키지 칩 20개 전달 (추가 칩 필요시 별도 협의)



〈 대표 공정별 Scope 이미지〉

〈 칩 다이싱 〉

〈 Bare-Die 〉



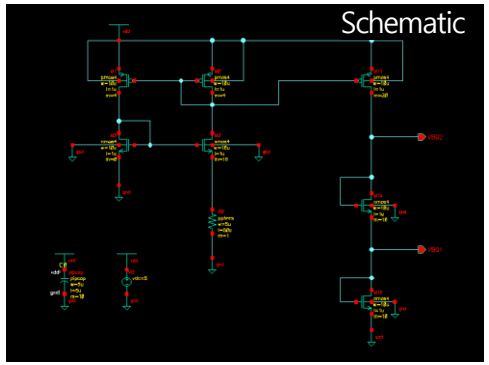
〈 패키지(28-Pin SOP) 칩 〉

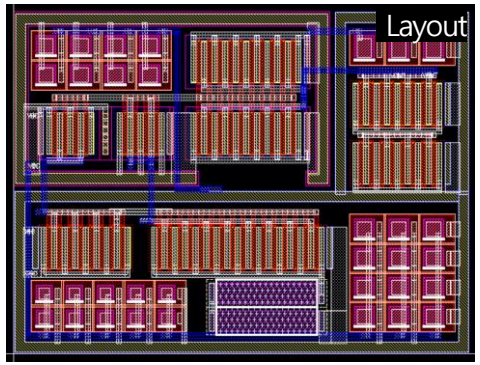
04. 내 칩(My Chip) 제작 서비스

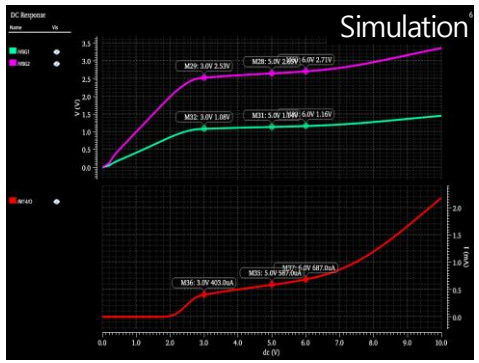
MPW 특성 (표준 IC)

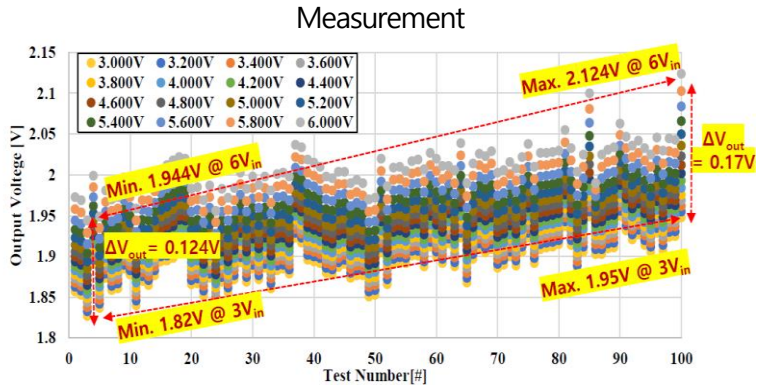
▣ Voltage Reference: CMOS의 VT 이용 Current Source 설계, 소자 특성(DC) 확인

→ V_{in}=3~6V, Simulation V_{out}=2.06V ~ 2.19V, 측정 V_{out}(avg.)=1.9V ~ 2.0V (Simulation과 차이 ~0.15V), 수율 100% (100칩 평가)

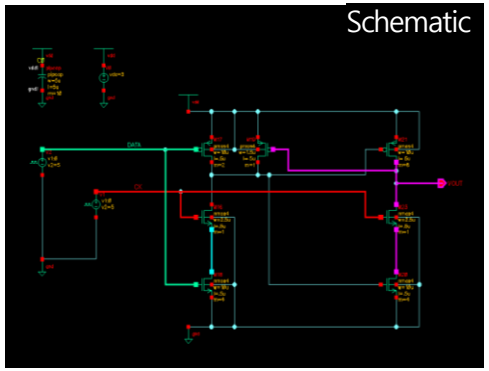


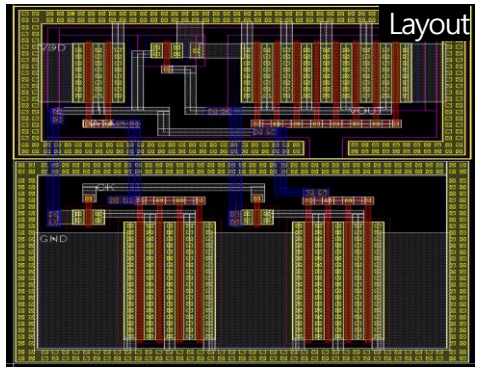


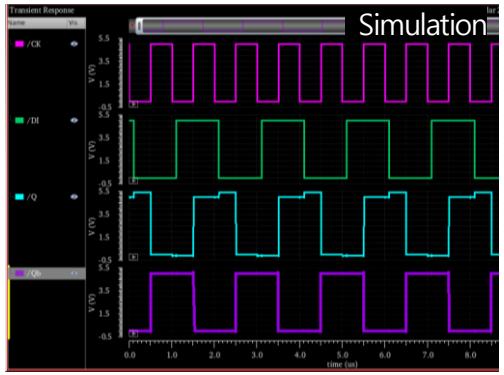




▣ Half D Flip-Flop: 동작속도 평가로 소자의 AC 특성 확인







→ Delay Time, Rising/Falling Time 평가
(Model Parameter, PEX 반영 예정)

→ Timing 측정 결과 Simulation과 일치 (C대)

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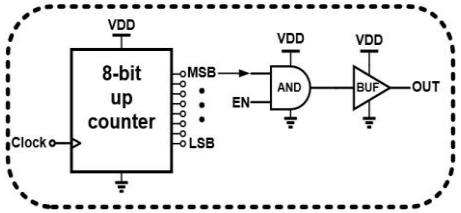
04. 내 칩(My Chip) 제작 서비스

2023년 MPW 사례 (1)_C대학교

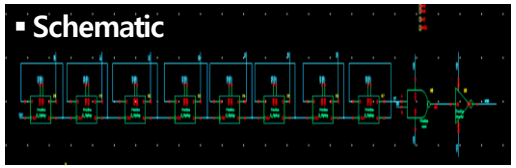
- 설계명: 산학 밀착형 T.O.P. 인재양성 시스템반도체 설계 인력양성을 위한 칩 설계
- 팀수(학생수): 23팀(68명), 학부3~4학년
- 4:1 MUX 및 그룹별 PAD 활용, 다수 설계팀을 한 칩으로 구현 → 16팀 MPW 칩 동작 확인, Timing 측정값 시뮬레이션과 유사

<팀별 8비트 카운터 설계>

▪ Block Diagram

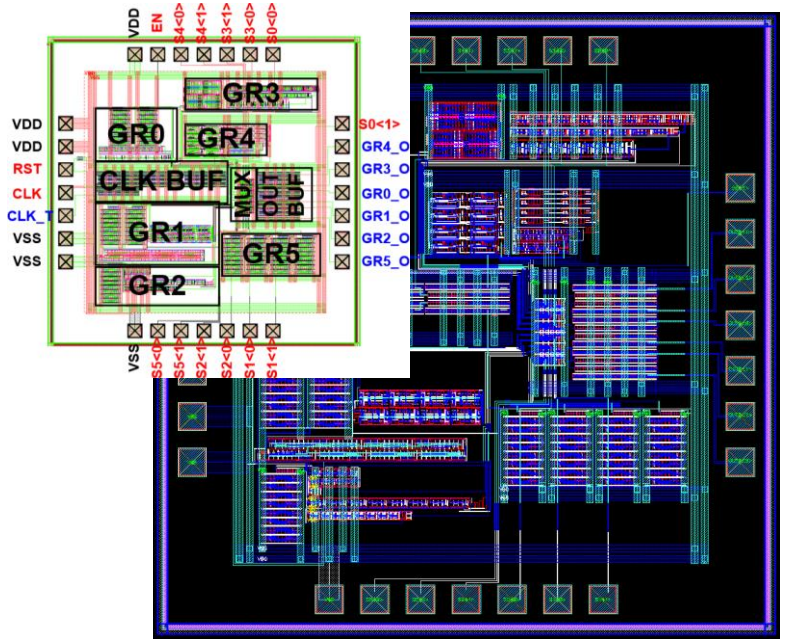


▪ Schematic

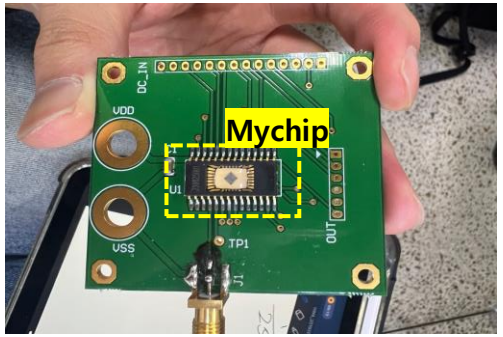


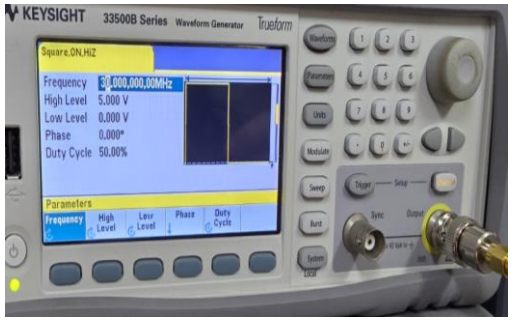
▪ Layout

<23팀 → 1칩 구성>



< MPW 칩 평가 >





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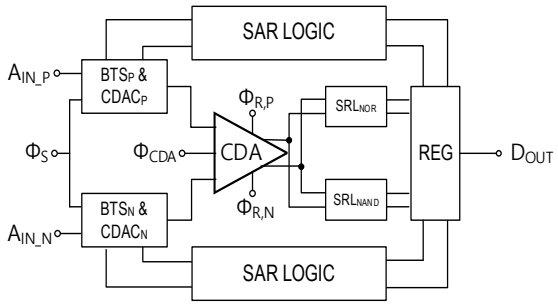
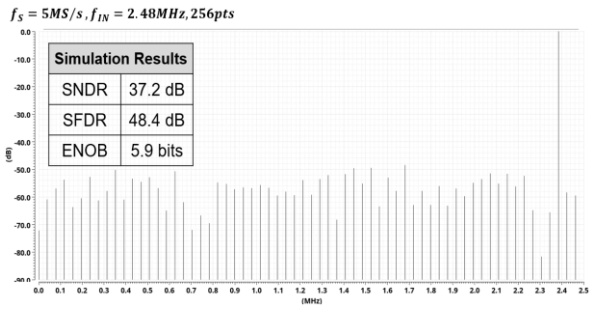
04. 내 칩(My Chip) 제작 서비스

2023년 MPW 사례 (2)_J대학교

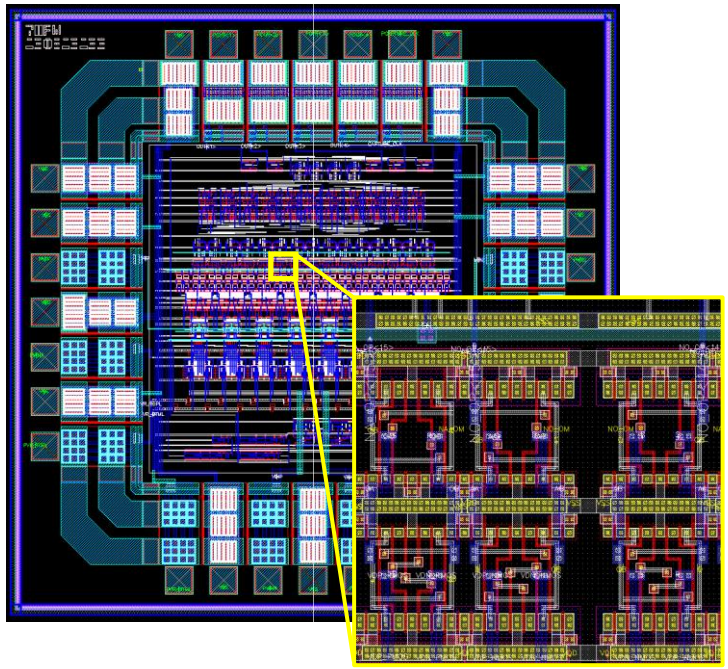
- 설계명: 상보 증폭기를 이용한 고속 데이터 변환기 개발 (A 6 bits SAR ADC with a Complementary Dynamic Amplifier)
- 팀수(학생수): 1팀(3명), 학부4학년
- 집적도가 높은 Mixed Mode (Analog + Digital) CMOS IC 설계 및 평가 → 양호한 MPW 칩 특성 확인

회로 설계 및 시뮬레이션



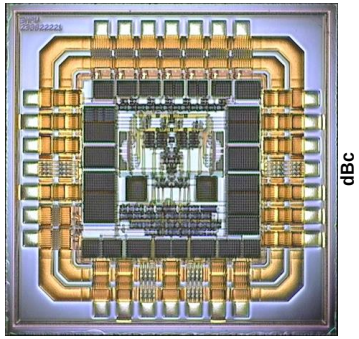


Layout

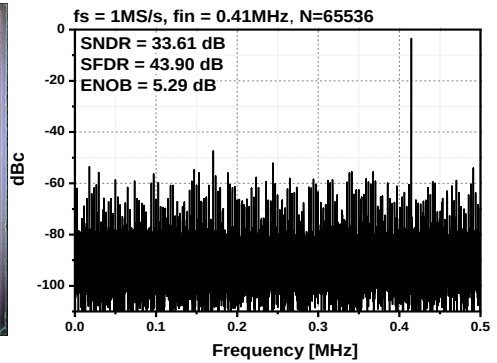


MPW 칩 평가

- My Chip Bare Die



- ADC 평가 결과



	시뮬레이션	실제 측정
전원 전압	5 V	5 V
전력 소모	4.97 mW	2.37 mW
sampling 주파수	5 MS/s	1 MS/s
SNDR	37.2 dB	33.61 dB
SFDR	48.4 dB	43.90 dB
ENOB	5.9 bits	5.29 bits

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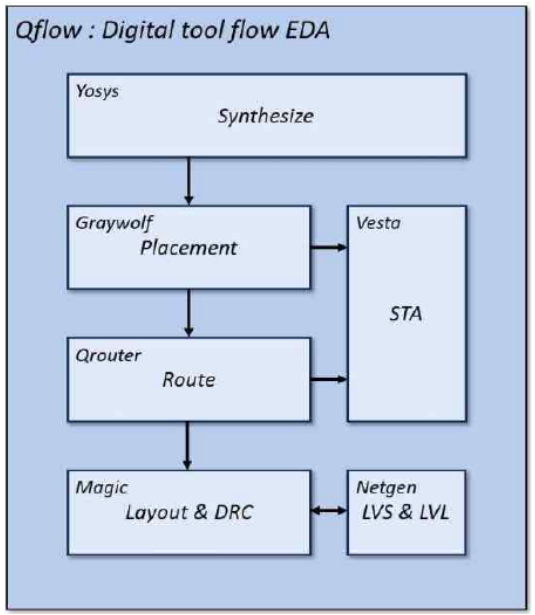
04. 내 칩(My Chip) 제작 서비스

2023년 MPW 사례 (3)_K대학교

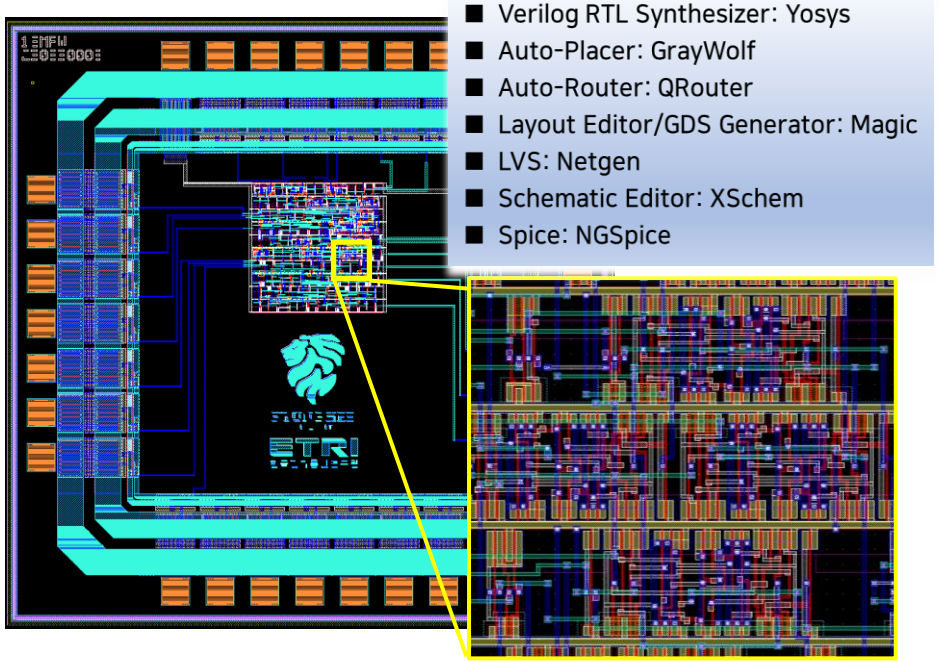
- 설계명: 부스 알고리즘 8비트 곱셈기(Booth Multiplier) 설계
- 팀수(학생수): 1팀(3명), 학부3학년
- Open Source Tool 사용, 제공 PDK를 활용하여 Standard Cell 구현 후 Digital IC 설계 → GPIO 변환 Error로 칩 동작 실패, 2024년 MPW 재 시도

(※ Open Source Tool 설계 강좌: 모아팹 MPW_My Chip 커뮤니티, 또는 https://fun-teaching-goodkook.blogspot.com/2024/07/mpw.html)

디지털 IC 설계 Flow



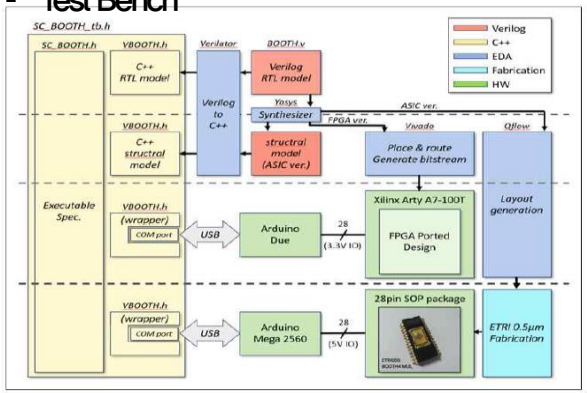
디지털 IC 설계



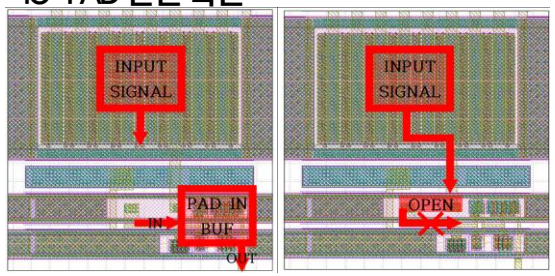
- Verilog RTL Synthesizer: Yosys
- Auto-Placer: GrayWolf
- Auto-Router: QRouter
- Layout Editor/GDS Generator: Magic
- LVS: Netgen
- Schematic Editor: XSchem
- Spice: NGSpice

MPW 칩 평가

- Test Bench



- IO-PAD 단선 확인



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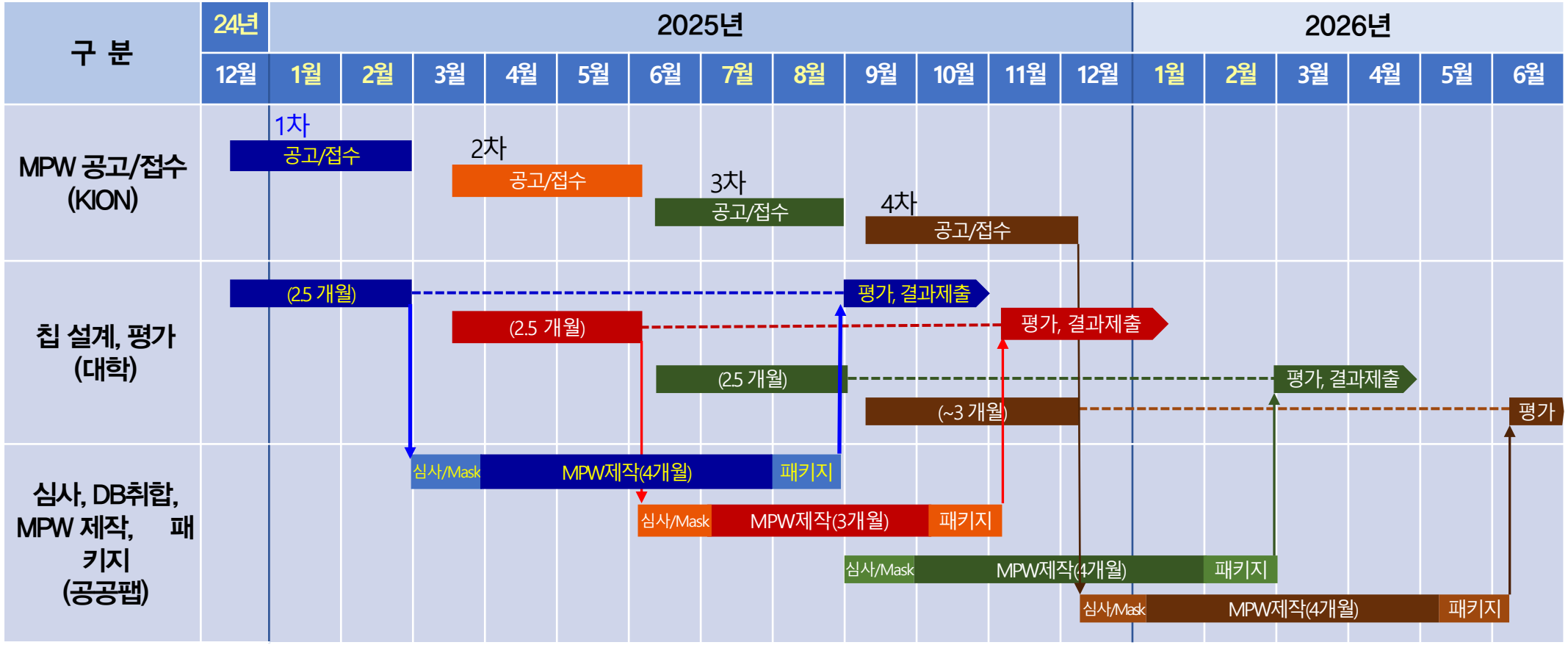
04. 내 칩(My Chip) 제작 서비스

2025년『내 칩 (My Chip) 서비스』일정(안)

- ✓ MPW 공고/접수: 총 4회, 대학 교육일정 (봄/여름/가을/겨울 학기)
- ✓ MPW 6회 제작 : SNU → ETRI → DGIST → ETRI → SNU → ETRI



*2025년 2차 "내 칩 서비스"의 MPW TAT 3개월 시범 진행 예정

감사합니다

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